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Renewable energy system using Multi-level Inverters Technology

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A thesis submitted as Capstone Project for the Bachelor Science of Technology with Electronic at UniSIM.

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Abstract

Due to the shortfall of fossil fuels in the near future, development of alternative source of energy is needed. The rapid growth in consumption of electric power has always been a concern for every country. This has lead to the increase concern and emphasis on the research and development of alternative sources of energy.

In this project, an inverting system for renewable energy application will be developed using the cascaded H-bridge multilevel inverter technology, which is able to synthesize a desired ac voltage from several levels of dc voltages. Solar energy is the form of renewable energy source in the system. In real world, Photovoltaic (PV) cells can be used to generate dc voltages and will be converted to an ac voltage by the multilevel inverter.

A cascaded H-bridge multilevel inverter using DC voltages as Photovoltaic (PV) cells model will be built using the MATLAB software. It will be used to investigate and verify the quality of the ac output voltage, harmonic content of the output voltage and effects of different switching scheme.

This project investigates several control techniques applied to the cascaded H-bridge multilevel inverter in order to ensure an efficient voltage utilization and better harmonic spectrum. Computer simulation results using MATLAB program are reported and discussed together with a comparative study of the different control techniques of the cascaded multilevel inverter.

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1. Introduction

1.1 Overall objective

The overall objective of this project is to develop an inverting system for renewable energy application using multilevel inverter technology, which is able to synthesize a desired ac voltage from several levels of dc voltages. This ac voltage can be used to power equipment that is not critical in operation.

Solar energy (photovoltaic cells) is used as the form of renewable energy source.
Pulse-width modulation switching technique will be implemented in this project.

The main focus will be a simulation study of the cascaded H-bridge multilevel inverter using separated DC sources (SDCSs) as a photovoltaic cell and a resistance/inductance load. Cascaded H-bridge model with multiple modules will be built using MATLAB simulink. It will be used to investigate and verify the quality of the ac output voltage, harmonic content of the output voltage and effects of different switching scheme.

1.2 Background

Energy is essential to the society to ensure our quality of life and to underpin all other elements of our economy. Renewable energy technologies offer the promise of clean, abundant energy gathered from self-renewing resources such as the sun, wind, earth and plants. [6]

Renewable energy technologies offer important benefits compared to those of conventional energy sources. Renewable energy resources are abundant: worldwide, 1000 times more energy reaches the surface of the earth from the sun than is released today by all fossil fuels. [6]

The economic prosperity of a nation is directly linked to abundant and secure supplies of energy. To maintain this wealth and success, it will be imperative to ensure that fuel supplies can be provided in the future, and as our dependency on fossil fuels will inevitably need to be reduced. [7]

Photovoltaic energy source is being increasingly recognized as cost effective generation source in small isolated power system (SIPS) primarily supplied by costly diesel fuel. [8] DC source is only available from PV cells, thus a dc to ac converter is needed.

Cascaded H-bridge Multilevel Inverter has been receiving wide attention due to its numerous advantages as a dc/ac interface. The advantages are [9] [10] [11]:

- Requires the least number of components compare to other multilevel inverters.
- Each inverter is in modular layout. Therefore able to add-on or replaced when necessary.
- Can generate almost sinusoidal waveform voltage while only switching one time per fundamental cycle.
- Able to make direct parallel or series connection to medium and high voltage power system without any transformer.
- High efficiency due to minimum switching frequency.
- Eliminate the use of transformer.

2. Investigation on Inverter Topologies

Multilevel voltage source converters are emerging as a new breed of power converter options for high-power applications. The multilevel voltage source converters typically synthesize the staircase voltage wave from several levels of dc voltages. There are some multilevel voltage source converters which are 1) diode-clamp, 2) flying capacitors, and 3) cascaded-inverters with separate dc sources. [9]

In this section, Conventional Inverter and different multilevel converters topologies shall be discuss.

2.1 Conventional Inverter [15]

2.1.1 Half-Bridge Inverter

As shown in Fig 2.1, half-bridge inverter consists of 2 switches, 2 diodes and 2 dc sources. This inverter works where SW1 is 'ON', SW2 is 'OFF' and vice-versa. $+V_{dc}/2$ is generated at the output when SW1 is 'ON', SW2 is 'OFF' and $-V_{dc}/2$ is generated when SW1 is 'OFF', SW2 is 'ON'.

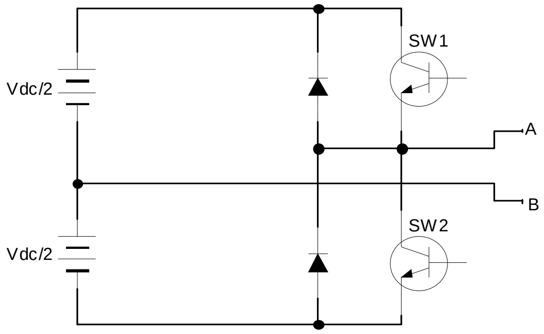


Fig 2.1 Half-bridge inverter

2.1.2 Full-Bridge Inverter

As shown in Fig 2.2, full-bridge inverter consists of 4 switches, 4 diodes and 2 dc sources. It operates in two modes.

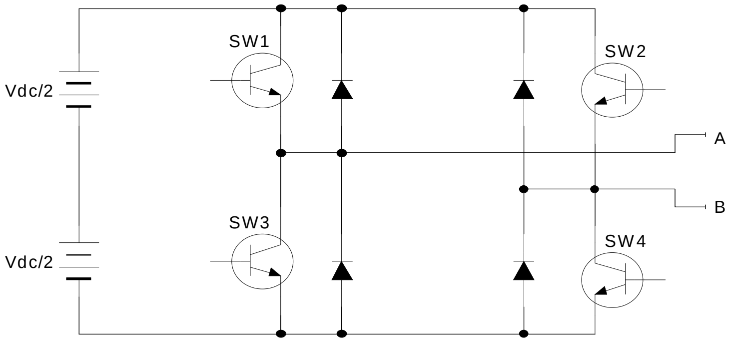


Fig. 2.2 Full-bridge inverter

First mode of operation, +Vdc is generated when SW1 & SW4 are 'ON' and –Vdc is generated when SW2 & SW3 are 'OFF'.

Second mode of operation, 0V is generated when SW1 & SW2 or SW3 & SW4 are 'ON'. This mode of operation is the fundamental building block for Cascaded H-bridge multilevel inverter. Fig 2.3 & Fig 2.4 shows the output voltage for the first and second mode of operation.

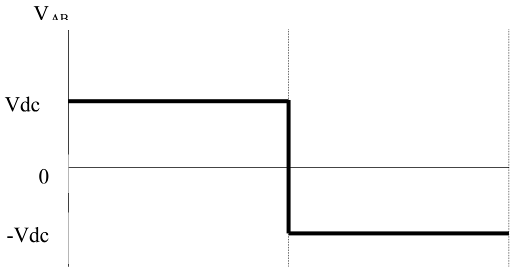


Fig. 2.3 First mode

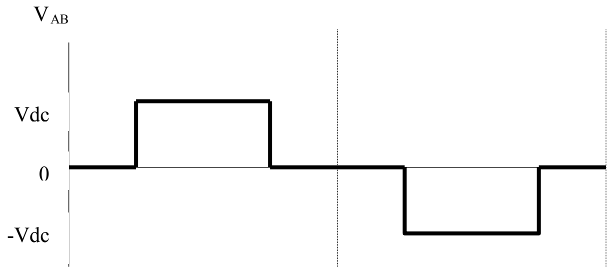


Fig. 2.4 Second mode

2.2 Multilevel Inverter

A brief introduction and description of each type of inverter is discussed as follow.

2.2.1 Diode-Clamp Multilevel Converters [9]

Basic Principle:

An m-level diode-clamp converter typically consists of m – 1 capacitors on the dc bus and produces m levels of the phase voltage. Fig. 2.5 shows a single-phase full bridge five-level diode-clamp converter in which the dc bus consists of four capacitors, C_1, C_2, C_3 and C_4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes.

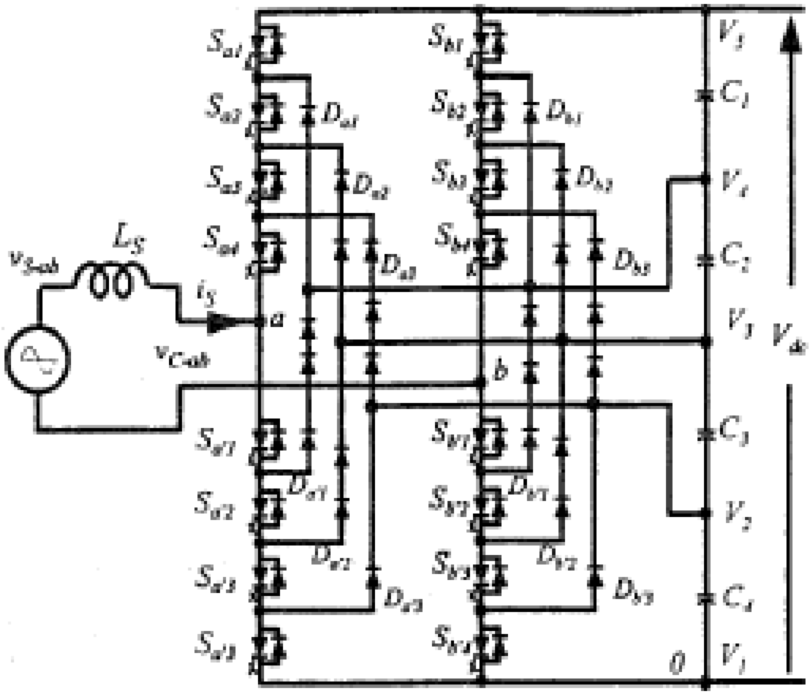
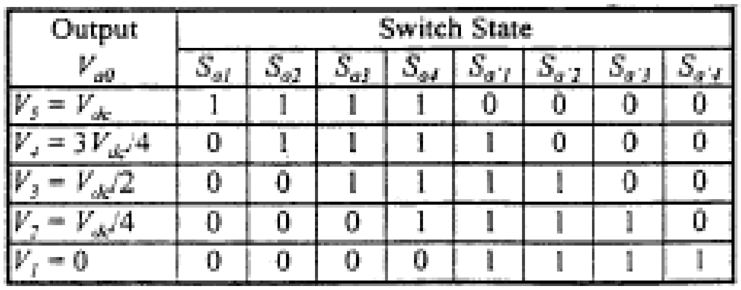


Fig. 2.5 A diode-clamp 5-level converter circuit diagram

Table 1 lists the voltage levels and their corresponding switch states. State 1= ‘ON’ and State 0=’OFF’.

TABLE I
DIODE-CLAMP 5-LEVEL CONVERTER VOLTAGE
LEVELS AND THEIR SWITCH STATES



Output V_{a0}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3 = V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2 = V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

Fig. 2.6 shows phase and line voltage waveforms of the 5-level converter. The resulting line voltage is a 9-level staircase wave. This implies that an m-level converter has an m-level output phase voltage and a (2m-1)-level output line voltage.

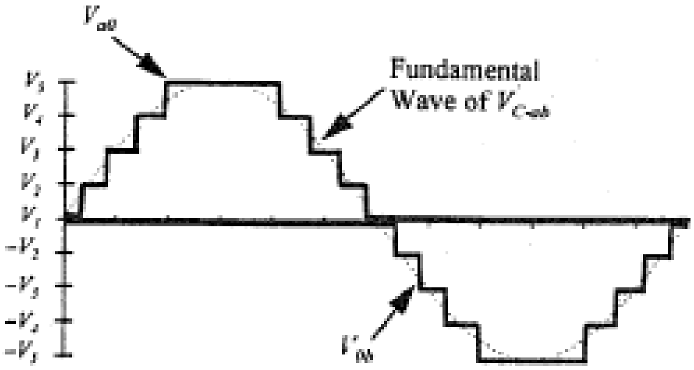


Fig. 2.6 Phase and line voltage waveform of a 5-level diode-clamp voltage source converter

The clamping diodes need to have different voltage ratings for reverse voltage blocking. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the numbers of diodes required for each phase will be (m-1) X (m-2). This equation shows a quadratic increase in m. If m is high, the number of diodes required will be impractical to implement.

Advantages of a diode-clamp multilevel voltage source converter

- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Efficiency is high because all devices are switched at the fundamental frequency.
- Reactive power flow can be controlled.
- The control method is simple for a back-to-back intertie system.

Disadvantages of a diode-clamp multilevel voltage source converter

- Excessive clamping diodes are required when the number of levels is high.
- It is difficult to do real power flow control for the individual converter.

2.2.2 Flying-Capacitors Multilevel Converters [9]

The voltage level defined in the flying-capacitor converter is similar to that of the diode-clamp type converter. The phase voltage of an m-level converter has m levels including the reference level, and the line voltage has (2m-1) levels.

The working principle is based on charging each capacitor to a different voltage level. The different in the magnitude of the voltage level between two capacitors will regulate the size of the output voltage at the terminal.

Fig. 2.7 shows the single-phase full-bridge flying-capacitor based 5-level converter.

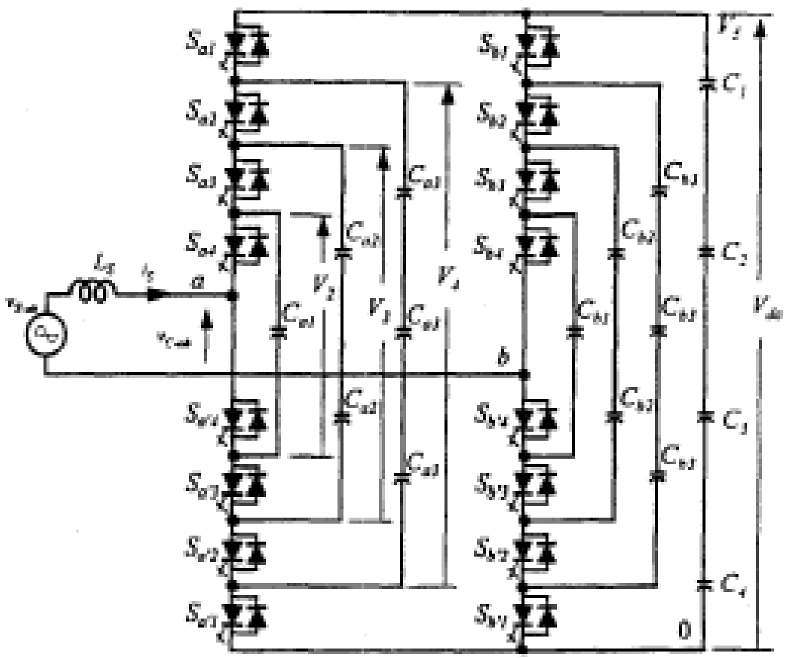
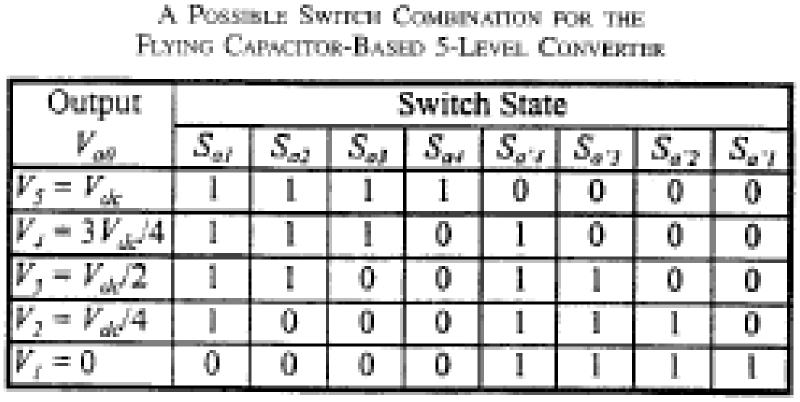


Fig. 2.7 A flying-capacitor based 5-level converter circuit diagram

Table 2 lists the voltage levels and their corresponding switch states.

Table 2



A POSSIBLE SWITCH COMBINATION FOR THE FLYING CAPACITOR-BASED 5-LEVEL CONVERTER

Output V_{a0}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3 = V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2 = V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

Large number of storage capacitors is required. An m-level converter require a total of (m-1) x (m-2)/2 auxiliary capacitors per phase leg in addition to (m-1) main dc bus capacitors.

Advantages of a flying-capacitor multilevel voltage source converter

- Large amount of storage capacitors provides extra ride through capabilities during power outage.
- Provides switch combination redundancy for balancing different voltage levels.
- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Both real and reactive power flow can be controlled.

Disadvantages of a flying-capacitor multilevel voltage source converter

- An excessive number of storage capacitors are required when the number of converter levels is high.
- The inverter control will be very complicated, and the switching frequency and switching losses will be high for real power transmission.

2.2.3 Cascaded H-bridges Multilevel Converters [10]

A cascaded multilevel inverter consists of a series of H-bridge (single-phase full-bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, which may obtain from batteries, fuel cells, or solar cells.

Fig. 2.8 shows a single-phase structure of a cascade inverter with separate dc sources. Each separate dc source is connected to a single-phase full-bridge inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and –Vdc.

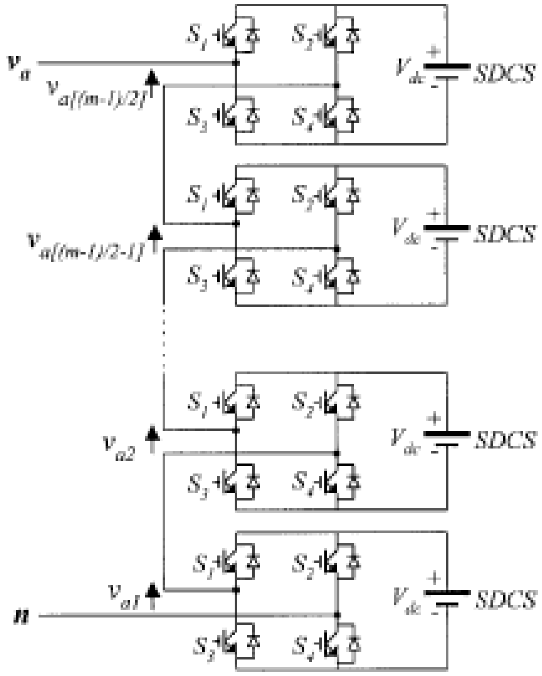


Fig. 2.8 Single-phase structure of a multilevel cascaded H-bridges inverter

The ac outputs of the inverters are connected in series such that the synthesized voltage waveform is the sum of the inverters outputs. The output phase voltage levels is defined by m = 2s+1, s = no. of dc sources.

Cascaded H-bridge Multilevel Inverter has been receiving wide attention due to its numerous advantages as a dc/ac interface. The advantages are [9] [10] [11]:

- Requires the least number of components compare to other multilevel inverters.
- Each inverter is in modular layout. Therefore able to add-on or replaced when necessary.
- Can generate almost sinusoidal waveform voltage while only switching one time per fundamental cycle.
- Able to make direct parallel or series connection to medium and high voltage power system without any transformer.
- High efficiency due to minimum switching frequency.

2.3 Comparison of the Topologies

Diode-Clamp Multilevel Inverters, Flying-Capacitors Multilevel Inverters and Cascaded H-bridges Multilevel Inverters are all suitable to be used as an interface in Photovoltaic application, due to the modular structure of PV arrays, to generate different DC voltage levels. Two main concerns in selecting a suitable inverter for the project are the components count used and the switching algorithm on the inverter topologies.

For Diode-clamped multilevel Inverter and Flying-Capacitors Multilevel Inverter, the number of semiconductor devices used for the circuit is very high. Both inverters devices count is greater than Cascaded H-bridges Multilevel Inverter. Therefore, the Cascaded H-bridges Multilevel Inverter is the most cost-effective.

Diode-clamped multilevel Inverter, the charging time for each capacitor is different, such a capacitor charging profile repeats every half cycle, this result in un-balanced capacitor voltage between different levels. Though it can be solved by complicated control algorithm, this will result in system complexity and cost penalties. For Flying-Capacitors Multilevel Inverter, when it involves real power conversions, the selection of a switch combination becomes very complicated in order to balance the capacitor charge and discharge. Each capacitor must be charged with different voltages as the voltage level increase.

Cascaded H-bridges Multilevel Inverter is the focus of this project due to its components required is the least to achieve the same number of voltage levels. The circuit layout is in modular structure, which means a faulty module can be replaced with another module without affecting the rest of the circuit. Whenever there’s a need to increase the output voltage, additional modules can be added. This means lower maintenance cost too.

2.4 Investigation on IGBT [12]

Power MOSFETs were used in medium or low voltage applications which require fast switching. Whereas bipolar power transistors, thyristors and GTOs were used in medium to high voltage applications which require high current conduction.
A power MOSFET allows for simple gate control circuit design and has excellent fast switching capability. But at 200V or higher, it has the disadvantage of rapidly increasing on-resistance as the breakdown voltage increases. The Bipolar power transistor has excellent on-state characteristics due to the low forward voltage drop, but its base control circuit is complex.

The IGBT has the combined advantages of power MOSFET and Bipolar power transistor.

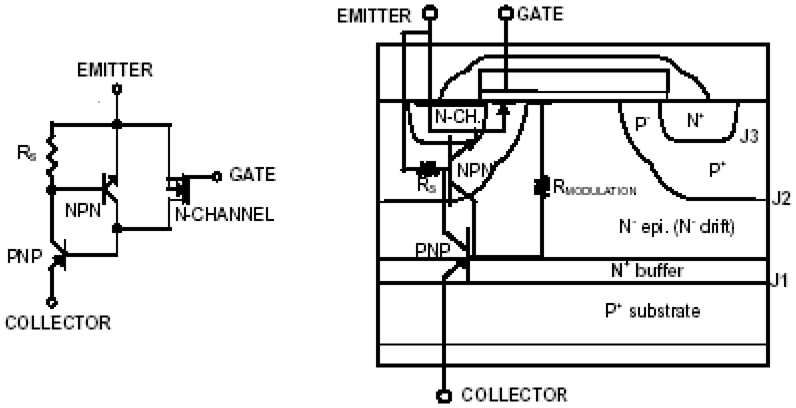


Fig 2.9 Equivalent Circuit for the IGBT and cross section of the IGBT Structure

Turn-on IGBT
Turn-on when the device is in the forward blocking mode, and the positive gate bias (threshold voltage), which is enough to invert the surface of P-base region under the gate, is applied, then an n-type channel forms and current begins to flow.

Turn-Off IGBT
Turn-Off when the gate voltage falls below the threshold voltage, the inversion layer cannot be maintained and the supply of electrons is blocked.

IGBT is chosen for the project due to the following reasons:

1) High forward conduction current density and low on-state voltage drop (not affecting the output voltage).
2) Low driving power and a simple drive circuit is enough due to the input MOS gate structure.
3) It has superior current conduction capability and excellent forward and reverse blocking capabilities.

3. FUNDAMENTAL OPERATION OF CASCADED H-BRIDGE

A cascaded H-bridge multilevel inverter consists of basic H-bridge modules connected in series. This section will explain the working principle of the H-bridge module and how the multilevel-cascaded modules are able to generate a single-phase ac out put voltage.

3.1 Structure of H-bridge Module and operation

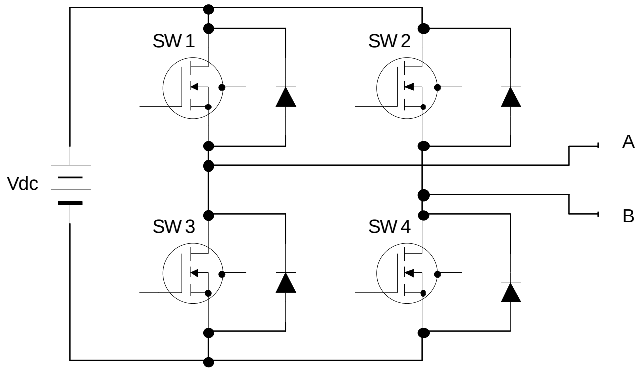


Fig. 3.1 Structure of a single H-bridge module

The structure of the single H-bridge module, as shown in Fig. 3.1, consist of a separate dc source (SDCS), four semiconductor switching devices and four diodes. The switching devices used are typically MOSFETs or IGBTs. IGBTs are chosen for this project due to High forward conduction current density, low on-state voltage drop, low driving power and fast switching response.

Switches, SW1, SW2, SW3 and SW4 are switched in 3 different sequences to generate output voltages across AB of the H-bridge module. The output voltage waveform is illustrated in Fig 3.2(e), which consist of three voltage levels, which are +Vdc, -Vdc and zero volt. To obtain +Vdc, switches SW1 and SW4 are turn 'ON'. To obtain –Vdc, switches SW2 and SW3 are turn 'ON'. To obtain zero volt, switches SW1 and SW2 or SW3 and SW4 are turn 'ON'. Fig 3.2(a-d) is the gate signal of the switching device SW1, SW2, SW3 and SW4 respectively. When the gate signal is at logic 1, it represents that the switching device is in conduction mode and a logic zero indicates that the device is not conducting.

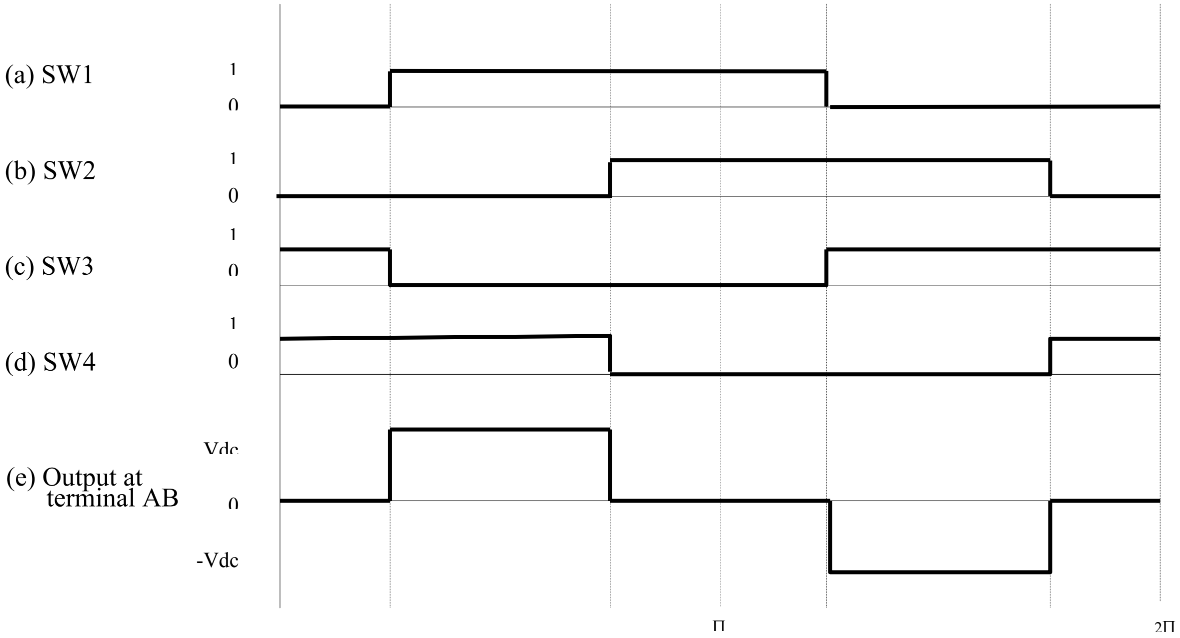


Fig 3.2 Switching devices gate signal and output voltage waveform

Sequence 1 (Fig 3.3):

- SW1 & SW 4 are turn 'ON'
- SW2 & SW3 are turn 'OFF'
- Resulted a +Vdc at terminal AB

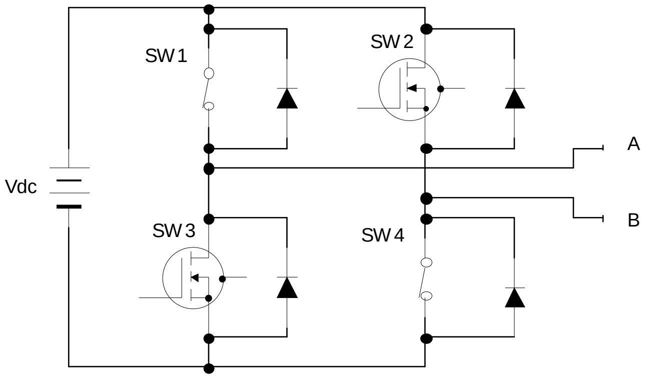


Fig 3.3 Switching sequence 1

Sequence 2 (Fig 3.4):

- SW2 & SW3 are turn 'ON'
- SW1 & SW4 are turn 'OFF'
- Resulted a -Vdc at terminal AB

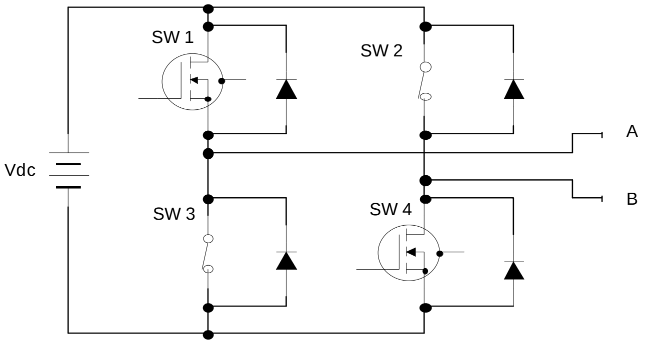


Fig 3.4 Switching sequence 2

Sequence 3 (Fig 3.5):

- SW1 & SW2 are turn 'ON' and SW3 & SW4 are turn 'OFF'. Alternately,
- SW3 & SW4 are turn 'ON' and SW1 & SW2 are turn 'OFF'.
- Resulted a zero volt at terminal AB

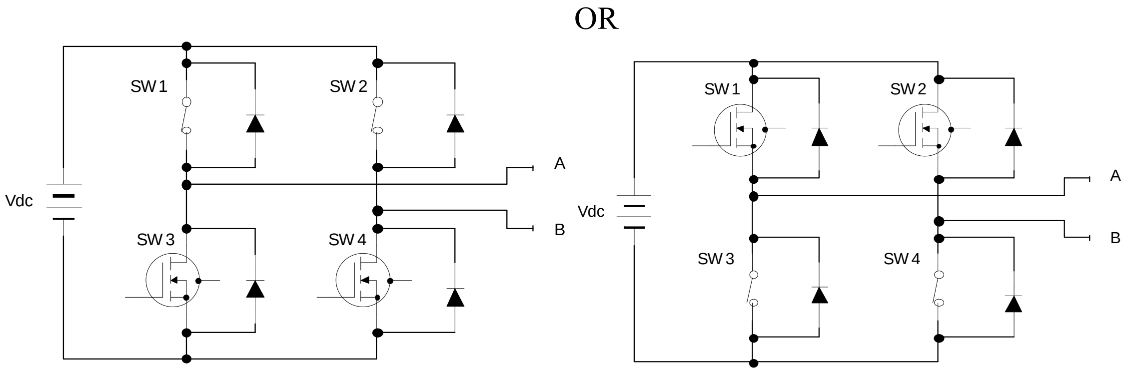


Fig 3.5 Switching sequence 3

3.2 Single-Phase Structure

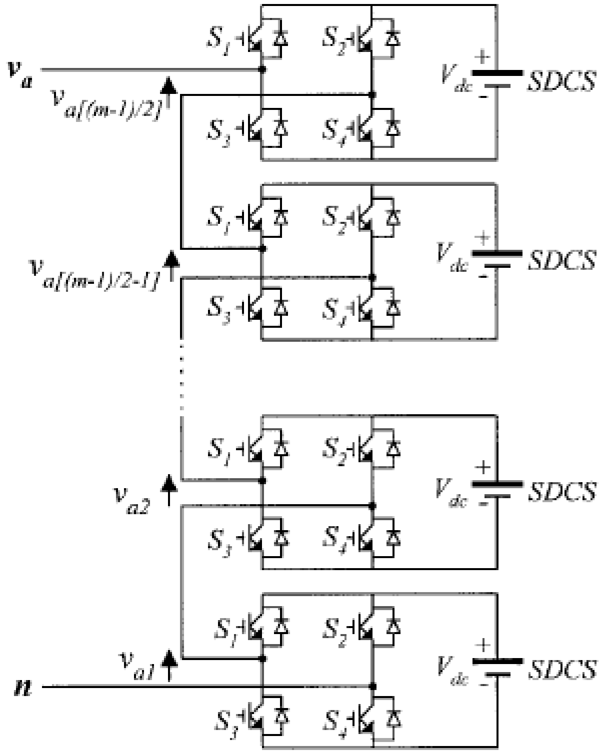


Fig 3.6 Single-phase structure of a multilevel cascaded H-bridges inverter

The cascaded H-bridge multilevel inverter single-phase structure in Fig 3.6 is constructed by connecting the H-bridge module in series [10]. The principle of operation is to synthesize the output voltage of each module to form a step-like ac voltage waveform across terminal Van.

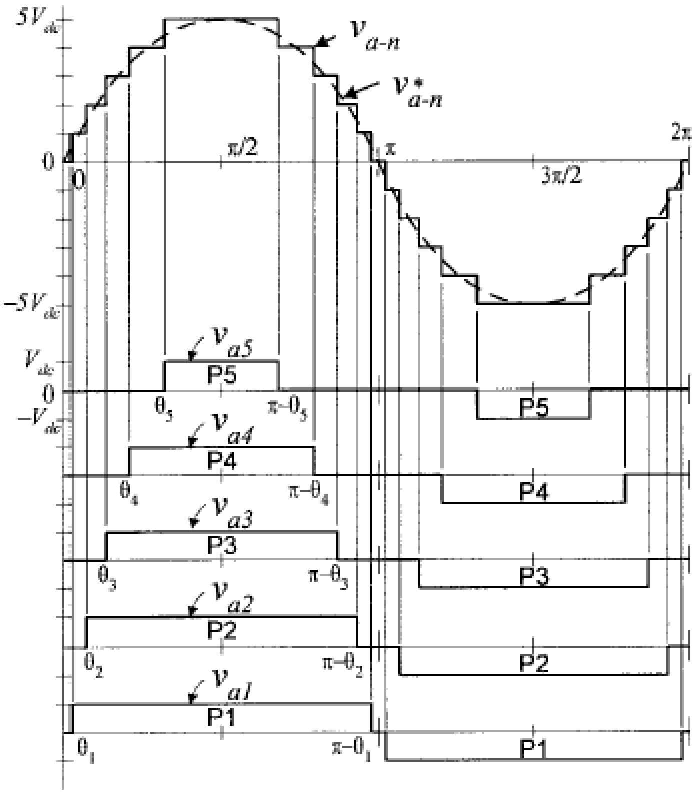


Fig 3.7 Synthesize output waveform at Van

Fig 3.7 shows the output waveform produced by summing up the inverter outputs. In general, the Van output voltage is produced by summing up the output voltage of each module with different duty cycle. The output voltage is almost sinusoidal. The greater the number of H-bridge modules in a single-phase structure, the more step the Van output voltage will be, therefore producing an ac waveform closer to a sinusoidal waveform.

The number of output phase voltage levels in a cascade inverter is defined by [10],

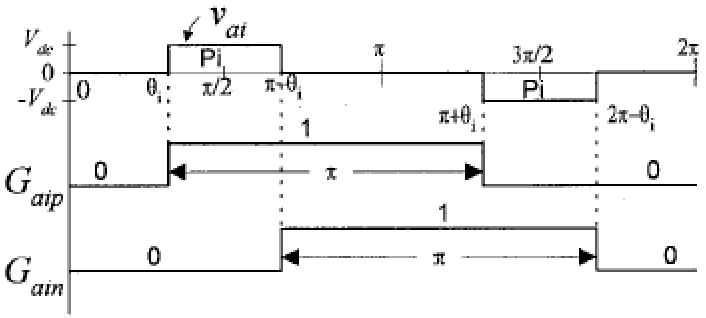
$$m=2s+1$$

Where s is the number of dc sources.

An example phase voltage waveform for an 11-level cascaded inverter with five SDSC's and five full bridges is shown in fig 3.7. The phase voltage is,

$$Van= Va1 + Va2 +Va3 + Va4 + Va5$$

The output voltage of the inverter is almost sinusoidal. Each H-bridge module generates a quasi-square waveform by phase shifting its positive and negative phase legs' switching timings. Fig 3.8 shows the switching timings to generate a quasi-square waveform.



G_{aip}, G_{ain}="0": Lower device on; "1": Upper device on.

Fig 3.8 Switching timing to generate quasi-square waveform

As explained in section 3.1, the switching timing chosen is due to the nature fundamental operation of the cascaded H-bridge inverter.

The input to the inverters will be assumed to be a dc voltage source. Such inverters are referred to as voltage source inverters (VSIs) [14].

The VSIs can be further divided into pulse-width-modulated inverters and Square-wave inverters.

1. Pulse-width-modulated inverters- In these inverters, the input dc voltage is constant in magnitude. Thus, the inverter must control the magnitude and the frequency of the ac output voltages. This is achieved by pulse-width-modulation (PWM) of the inverter switches. These inverters are called PWM inverters. There are various schemes to modulate the inverter switches to shape the ac output voltage to be as close to a sinusoidal waveform. This shall be discussed in the next section.

2. Square-wave inverters- In these inverters, in order to control the magnitude of the output ac voltage, the input dc voltage is controlled. Thus, the inverter has to control only the frequency of the output voltage. The output voltage is a square wave. These inverters are called square wave inverters. This shall be discussed in the next section

4. SIMULATION STUDIES ON DIFFERENT SWITCHING TECHNIQUES

Simulation studies of this project are done using MATLAB program. The circuit of the single phase H-bridge multilevel inverter is built using MATLAB.

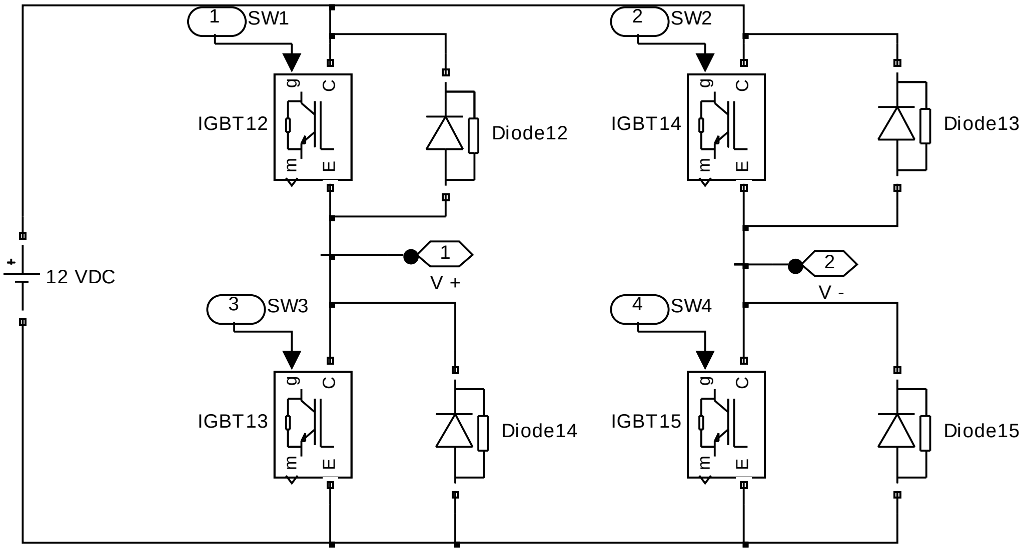


Fig 4.1 H-bridge circuit diagram in MATLAB

The simulation H-bridge model is using ideal components to eliminate all unnecessary errors due to the complexity of the circuit diagram. This circuit is format into a sub-system, H-Bridge Module, to reduce the space used in MATLAB.

4.1 Square wave switching scheme

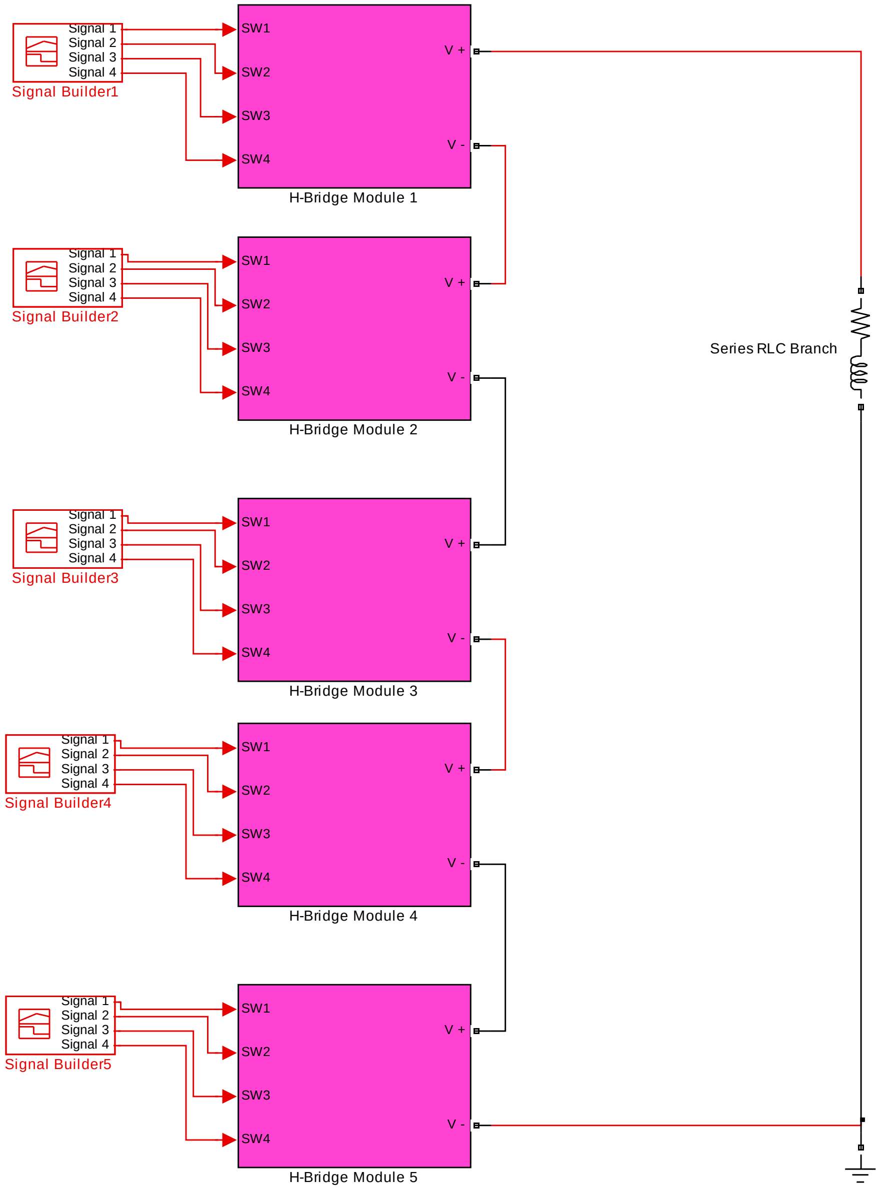


Fig 4.2 11-level cascaded H-bridge multilevel inverter

The simulated model in MATLAB of a 11-level cascaded H-bridge multilevel inverter is shown in Fig 4.2. Signal Builders are used to produce a bit-stream, a digital signal that produces a logic high to turn 'ON' the IGBT, and logic low to turn 'OFF' the switch. This is a form of square wave switching where the bit stream presents the gate signal of the switching technique. Another method of a square wave switching due to over modulation method shall be discussed in the next following section.

In fig 4.1, an ideal dc voltage source is used at the input to replace photovoltaic cell. A resistor and inductor are connected in series in the circuit as a load.

As mentioned in section 3.2, each H-bridge module generates a quasi-square waveform. For a square waveform such as the one depicted in fig 3.7, the Fourier transform for this waveform is as follows:

$$V(\omega t) = \frac{4V_{\mathrm{dc}}}{\pi} \sum_{n} [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \times \frac{\sin(n\omega t)}{n}, \quad \text{where } n = 1, 3, 5, 7, \cdots.$$

In fig 4.3, the conducting angles can Θ_1, Θ_2, Θ_3, Θ_4 and Θ_5 can be chosen such that the voltage total harmonic distortion is a minimum. These angles are chosen to cancel the predominant lower frequency harmonics [10]. For this 11-level cascaded H-bridge inverter case, the 5th, 7th, 11th and 13th harmonics can be eliminated with the appropriate choice of the conducting angles.

For example, using a modulation index of 0.8, choosing

$\Theta_1 = 6.57°$
$\Theta_2 = 18.94°$
$\Theta_3 = 27.18°$
$\Theta_4 = 45.15°$
$\Theta_5 = 62.27°$

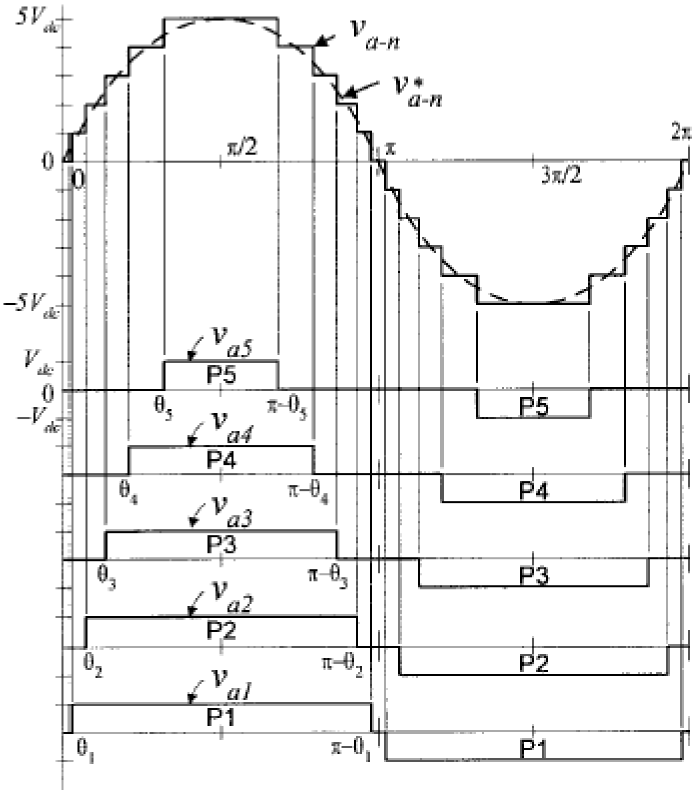


Fig 4.3 Synthesize output waveform at Van

If the inverter output is symmetrically switched during positive half cycle of the fundamental voltage to:

+Vdc at 6.57°,
+2Vdc at 18.94°,
+3Vdc at 27.18°,
+4Vdc at 45.14° and
+5Vdc at 62.24°

During negative half cycle,

-Vdc at 186.57°,
-2Vdc at 198.94°,
-3Vdc at 207.18°,
-4Vdc at 225.14° and
-5Vdc at 242.24°

The output voltage of the 11-level inverter will not contain the 5th, 7th, 11th, and 13th harmonic components. The output voltage is almost sinusoidal and it has less than 5% THD.

Simulation study in MATLAB is done on the above square-wave switching to verify the results.

In Fig 4.4(a), signal builder is used to produce the required quasi-square waveform. In order to produce the required H-bridge module output waveform, manual calculation had been made for individual signal from the signal builder. The calculation is base on section 3.1, fundamental operation of H-bridge inverter and the conducting angles chosen from this section.

Fig 4.4(b)-(e) shows the individual signal built in the signal builder. Fig 4.5(a) shows the output waveform from the H-bridge inverter module 1. All the presentation from fig 4.4 is base on H-bridge inverter module 1 from this 11-level multilevel inverter model from fig 4.2. Subsequent H-bridge module (module 2 to module 5) signal is built base on the explanation above.

As shown in fig 4.5(a), the output waveform is identical to P1 waveform of fig 4.3. The output waveforms of Signal Builder 2, Signal Builder 3, Signal Builder 4 and Signal Builder 5 in Fig 4.2 are shown in Fig 4.5(b)-(e). The output waveforms are identical to P2, P3, P4 and P5 of fig 4.3. Thus, the final output waveform from this 11-level Cascaded H-bridge multilevel inverter is shown in fig 4.6.

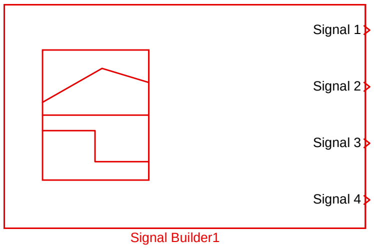


Fig 4.4(a) Signal Builder 1

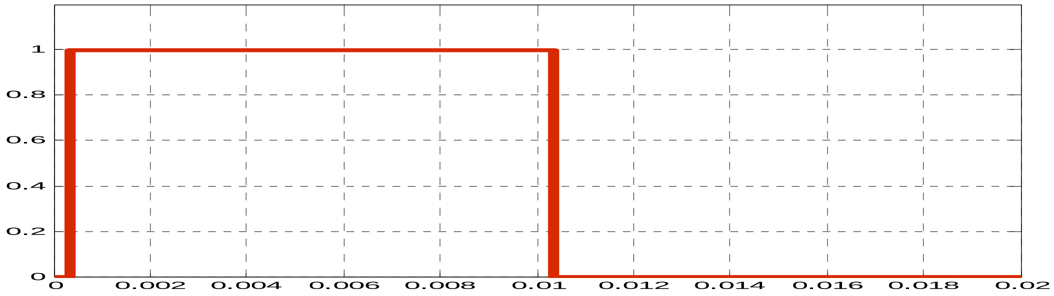


Fig 4.4(b) Signal 1 in Signal Builder 1

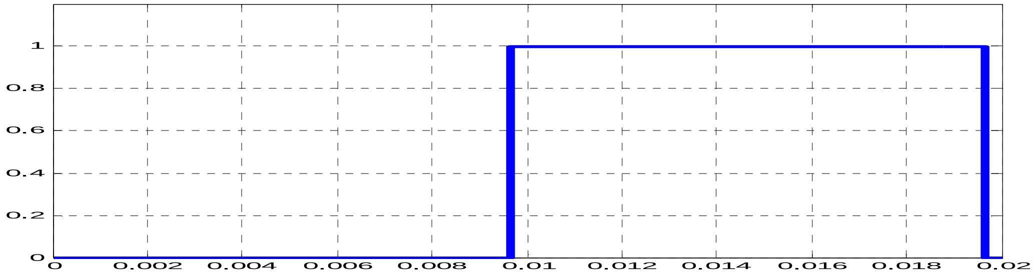


Fig 4.4(c) Signal 2 in Signal Builder 2

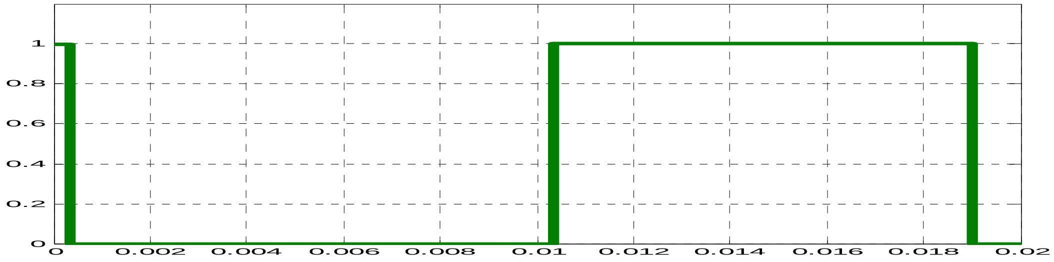


Fig 4.4(d) Signal 3 in Signal Builder 3

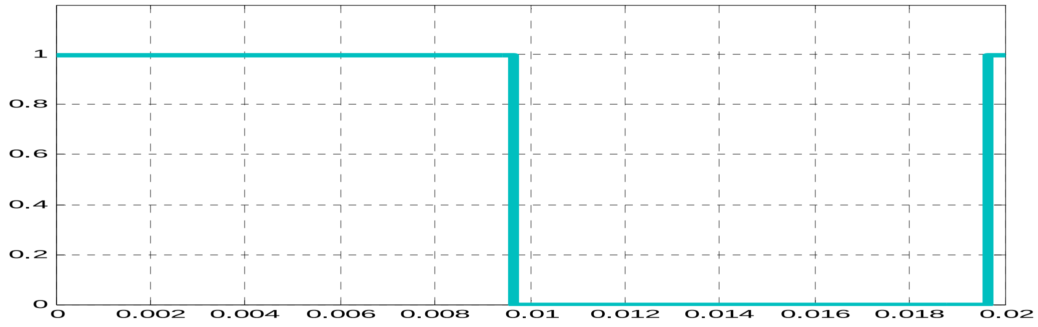


Fig 4.4(e) Signal 4 in Signal Builder 4

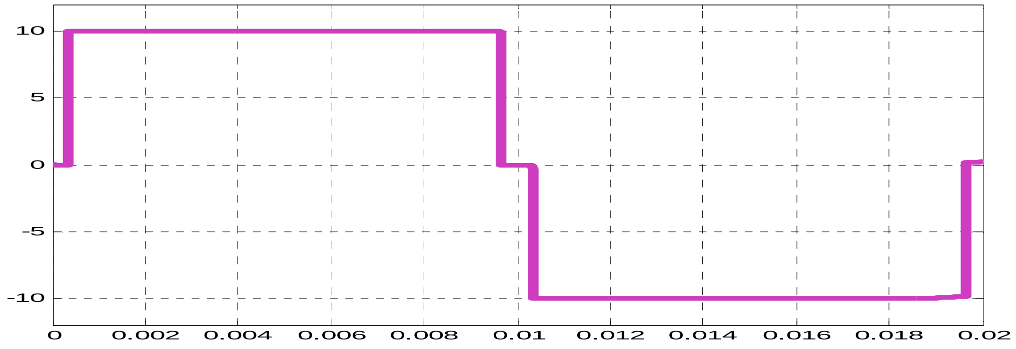


Fig 4.5(a) Output Signal from H-bridge module 1 (11-level model)

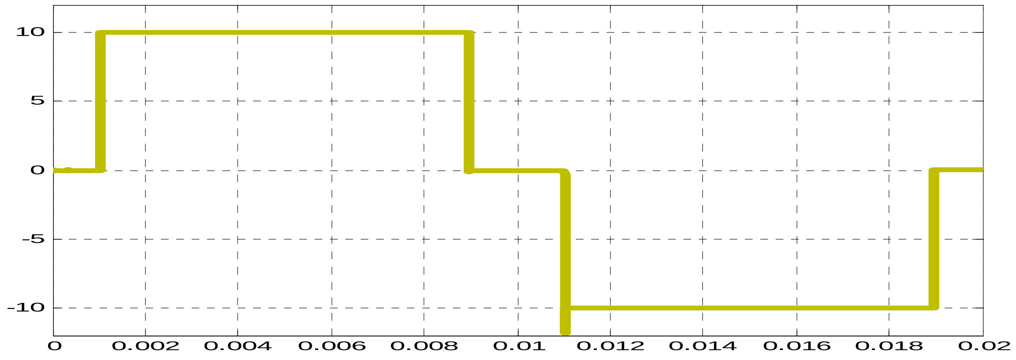


Fig 4.5(b) Output Signal from H-bridge module 2 (11-level model)

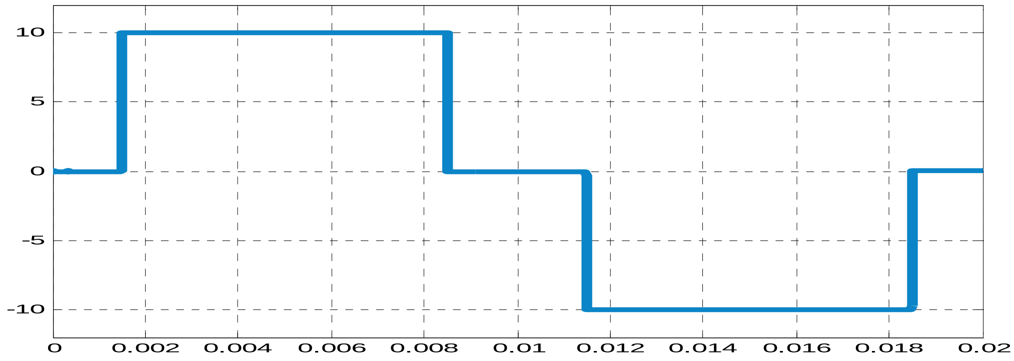


Fig 4.5(c) Output Signal from H-bridge module 3 (11-level model

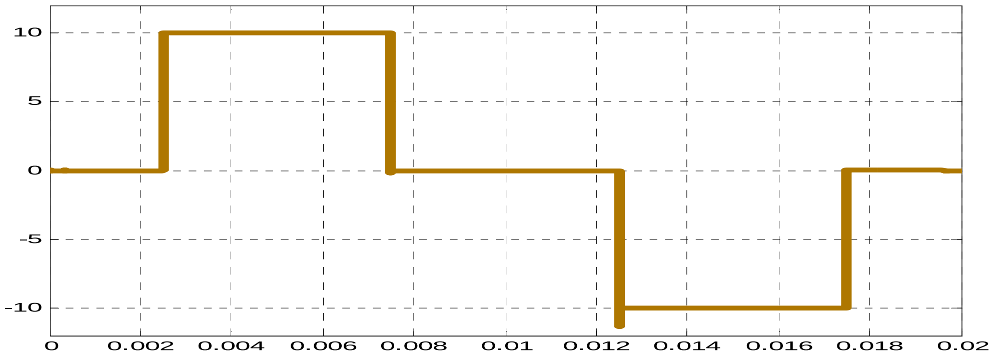


Fig 4.5(d) Output Signal from H-bridge module 4 (11-level model

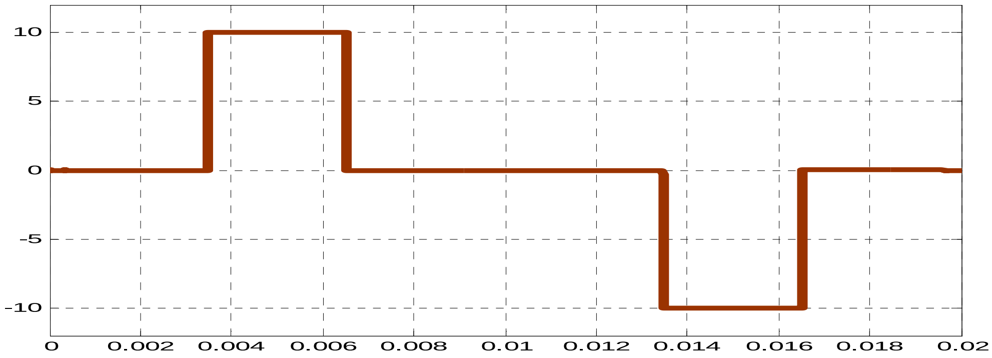


Fig 4.5(e) Output Signal from H-bridge module 5 (11-level model

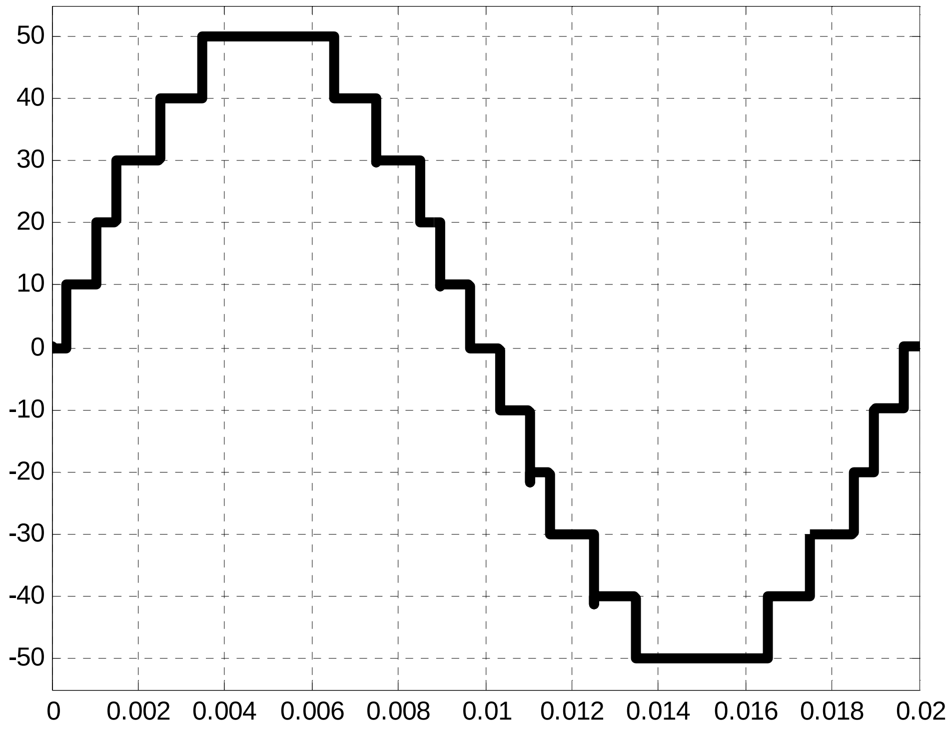
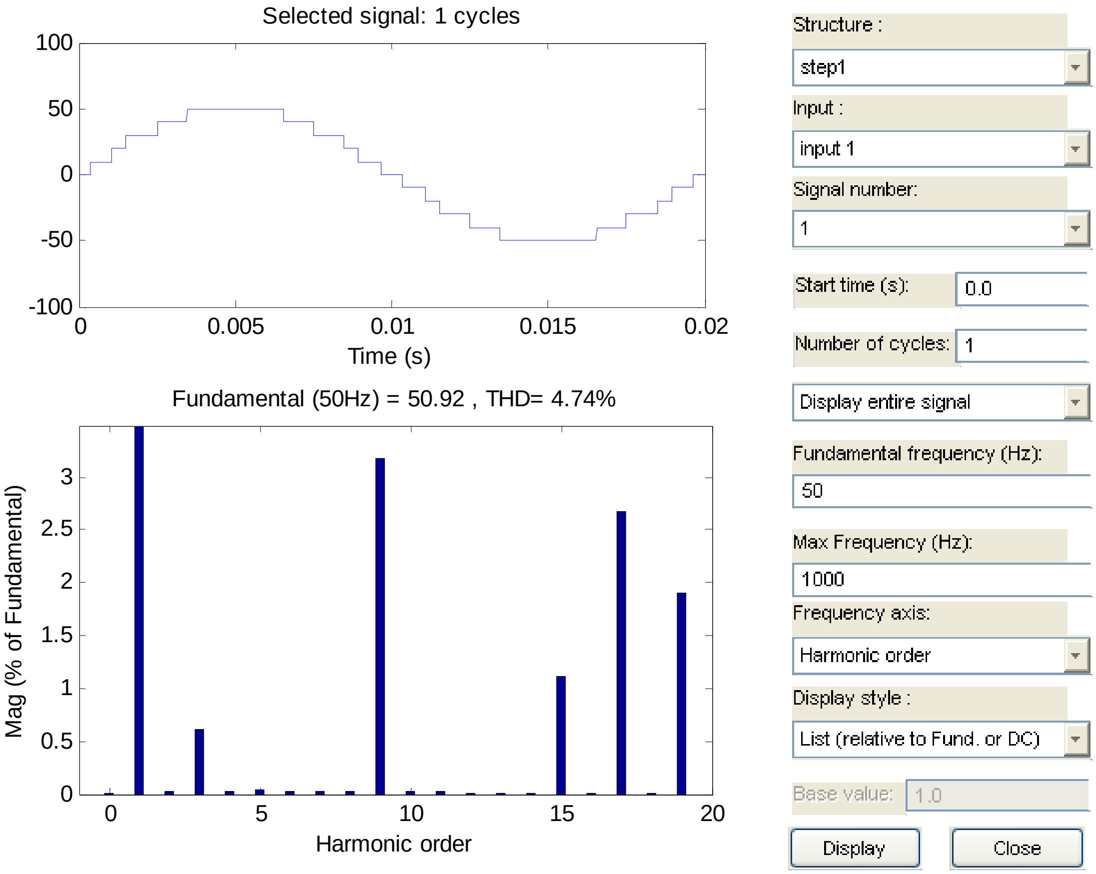


Fig 4.6 Final output waveform of 11-level multilevel inverter



Structure : step1

Input : input 1

Signal number: 1

Start time (s): 0.0

Number of cycles: 1

Display entire signal

Fundamental frequency (Hz): 50

Max Frequency (Hz): 1000

Frequency axis: Harmonic order

Display style : List (relative to Fund. or DC)

Base value: 1.0

Fig 4.7 FFT analysis of 11-level H-bridge multilevel inverter

FFT analysis is done on the output waveform as shown in fig 4.6 using Powergui in MATLAB. The total harmonic distortion is 4.74% which is lower than 5%. As expected, the output waveform of the 11-level inverter does not contain the 5th, 7th, 11th, and 13th harmonic components.

Total harmonic distortion (THD) is a measurement of the closeness in shape between a waveform and its fundamental component.

4.2 Pulse-width modulation (PWM) switching scheme

4.2.1 Introduction of Pulse-width modulation technique [14]

Basically, a control signal $V_{control}$ (constant or slowly varying in time) was compares with a repetitive switching frequency triangular waveform V_{tri}, in order to generate the switching signals. The average output voltage can be controlled by controlling the switch duty ratios.

For this project, the multilevel inverter output is to be sinusoidal with magnitude and frequency controllable. In order to produce a sinusoidal output voltage waveform at a desired frequency, a sinusoidal control signal at the desired frequency is compared with a triangle waveform as shown in fig 4.8.

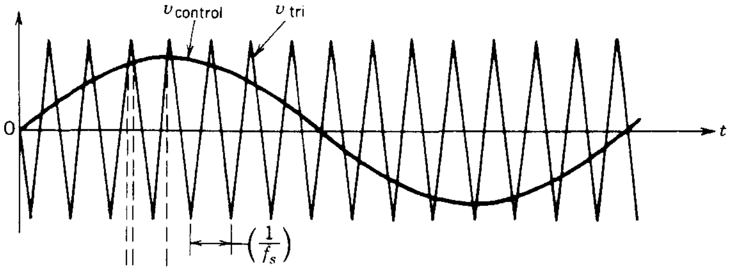


Fig 4.8 Control signal compares with triangle waveform

It is necessary to define a few terms before proceeding to the next sub-section.
The triangular waveform v_{tri}, called carrier signal in fig 4.8 is at a switching frequency f_{tri}, which establishes the frequency with which the inverter switches are switched. The triangular waveform is typically kept constant at peak amplitude of v_{tri}.

The control signal $v_{control}$ is used to modulate the switch duty ratio and has a frequency $f_{control}$, which is the desired fundamental frequency of the inverter voltage output. $f_{control}$ can be also called as a modulating frequency.

The amplitude modulation ratio $\mathbf{m_a}$ is defined as,

$$\mathbf{m_a} = \frac{V_{control}}{V_{tri}}$$

Where $V_{control}$ is the peak amplitude of the control signal, V_{tri} is the amplitude of the carrier signal.

The frequency modulation ratio $\mathbf{m}_f$ is defined as,

$$\mathbf{m}_f = \frac{f_{tri}}{f_{control}}$$

Where f_{tri} is the carrier frequency and $f_{control}$ is the modulating frequency.

In the project, the inverter switched is controlled by the comparison of $V_{control}$ and V_{tri}. When V_{tri} is greater $V_{control}$, a logic 1 is applied to the gate of the switching device. When $V_{control}$ is greater V_{tri}, a logic 0 is applied to the gate of the switching device

The selection of the carrier frequency and the frequency modulation ratio $\mathbf{m}_f$ is desirable to use as high a switching frequency as possible because of the ease in filtering harmonic voltages at high frequencies. The significant drawback is the switching losses in the inverter switches increase proportionally with the carrier frequency.

The amplitude modulation ratio controls the amplitude of the fundamental frequency voltage in two regions. In the case of $\mathbf{m_a \leq 1.0}$, the fundamental frequency voltage varies linearly with $\mathbf{m_a}$. In this range $\mathbf{m_a \leq 1.0}$, PWM pushes the harmonics into a high frequency range around the carrier frequency.

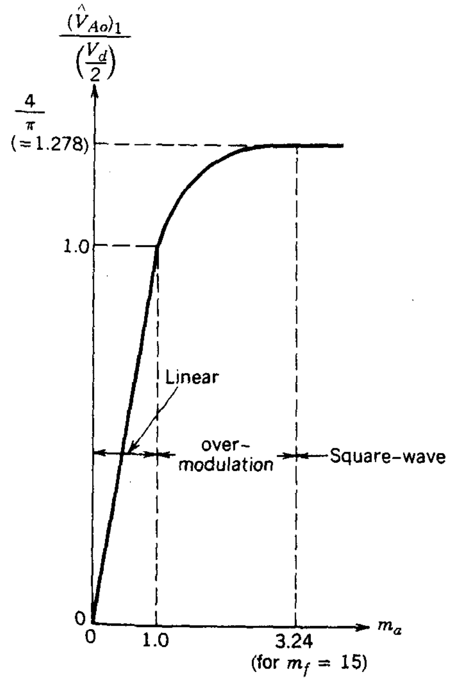


Fig 4.9 Voltage control by varying $\mathbf{m_a}$

It is also possible for an inverter to operate beyond the desired amplitude of the fundamental frequency voltage by increasing $\mathbf{m_a > 1.0}$, resulting in what is called overmodulation. Overmodulation causes the output voltage contains many more harmonics as compared to the linear region. With overmodulation, the amplitude of the fundamental frequency component does not vary linearly with the amplitude modulation ratio $\mathbf{m_a}$. The overmodulation is avoided in uninterruptible power supplies (UPS) because of a stringent requirement on minimizing the harmonics distortion in the output voltage. From Fig. 4.9, when the region of modulation gets large enough, the output voltage waveform will become a square wave. This will be verify in later part.

4.2.2 Pulse width modulation with Bipolar voltage switching [14]

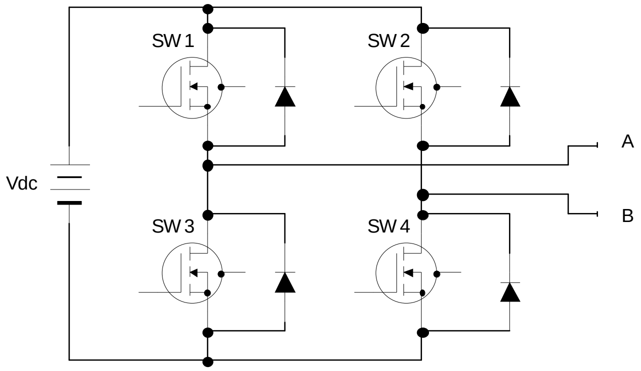


Fig 4.10 Single-phase full bridge inverter

Here, the diagonally opposite switches SW1 & SW4, SW2 & SW3 from the two legs in fig 4.10 are switch pair 1 and 2 respectively. Bipolar sinusoidal pulse width modulation is the simplest technique used in inverter technology. The gating signal of the four switching devices in each single phase full bridge inverter is generated, by comparing a sinusoidal control signal $v_{control}$ with a triangular signal (carrier) v_{tri} as shown in fig 4.11(a). The V_{AB} output voltage waveform is shown in fig 4.11(b). From fig 4.11(b), the output voltage V_{AB} switches between $-V_d$ and $+V_d$ voltage levels, that is the reason why this type of switching is called Pulse Width modulation Bipolar voltage switching.

The Bipolar sinusoidal pulse width modulation will be developed using MATLAB in the next sub-section.

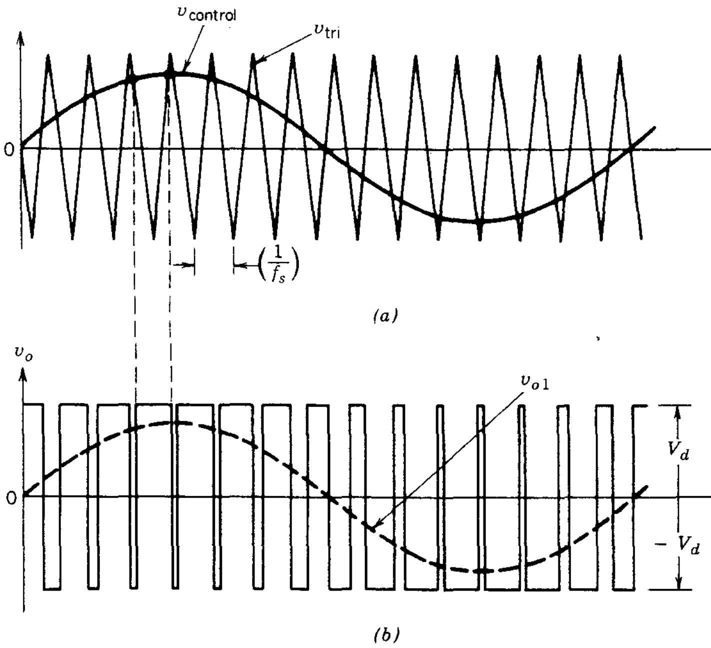


Fig 4.10 Bipolar sinusoidal Pulse Width Modulation

4.2.3 Simulation study on Bipolar sinusoidal Pulse width modulation with MATLAB

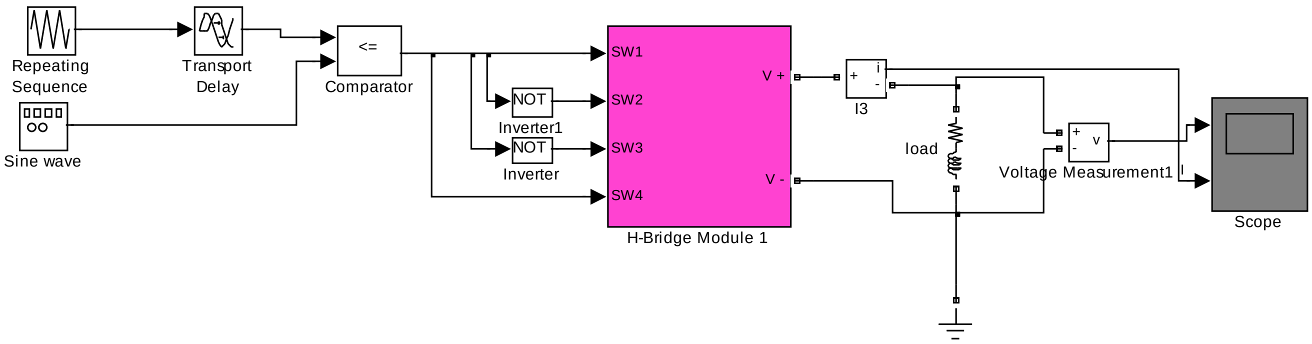


Fig 4.11 Bipolar switching in single phase H-bridge module

In fig 4.11, a Bipolar pulse width modulation single phase H-bridge with $\mathbf{m_a} = 0.8$ & $\mathbf{m}_f = 12$ is developed using MATLAB.

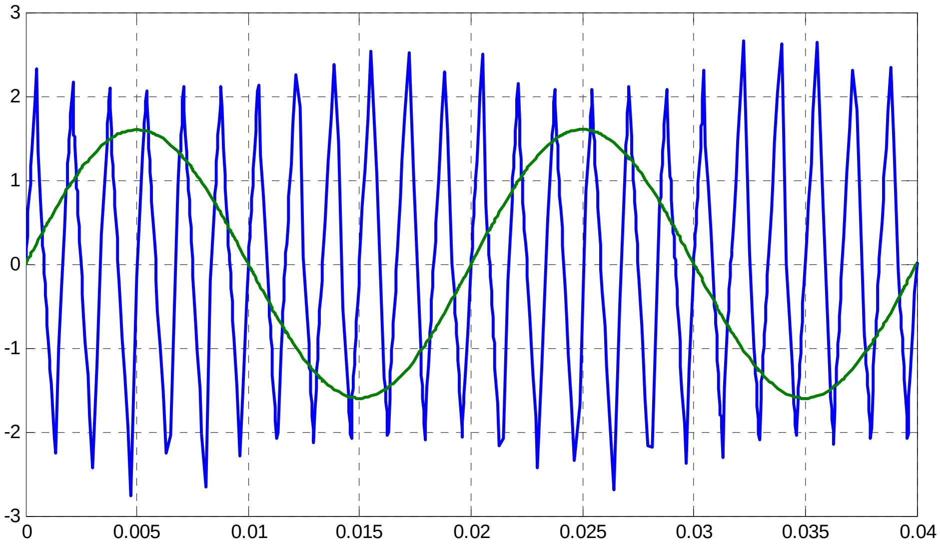


Fig 4.12 $V_{control}$ with a triangular signal (carrier) V_{tri}

In Fig 4.12, a control signal $v_{control}$ with amplitude 1.6V & frequency of 50Hz is compared with a carrier signal, v_{tri} triangle waveform with amplitude 2V & frequency of 600Hz. From the equation given in sub-section 4.2.1, $\mathbf{m_a}$ is calculated as 0.8 & $\mathbf{m}_f$ is calculated as 12.

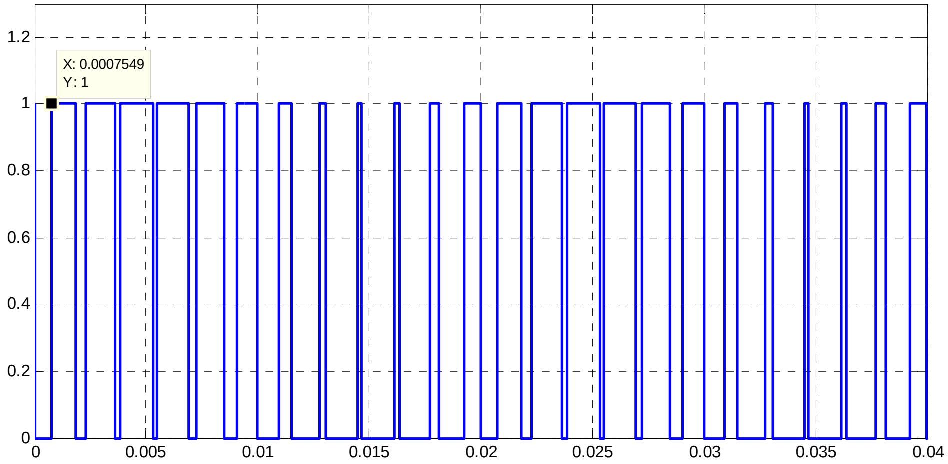


Fig 4.13 Gating signal from comparator applied to SW1

As shown in fig 4.13, a signal is generated out from the comparator after the triangle waveform is compared with the control signal (sine wave).

When $v_{control} > v_{tri}$, gating signal is 'ON'. This gating signal is applied to SW1 & SW4. An inverted gating signal is applied to SW2 & SW4. In this way, the switching devices are diagonally switch 'ON' and 'OFF'.

This technique only produced 2 levels of voltage at the output. As shown in fig 4.14, the output voltage is $+V_{dc}$ when SW1 & SW4 are turn on, and $-V_{dc}$ when SW2 & SW3 are turn on.

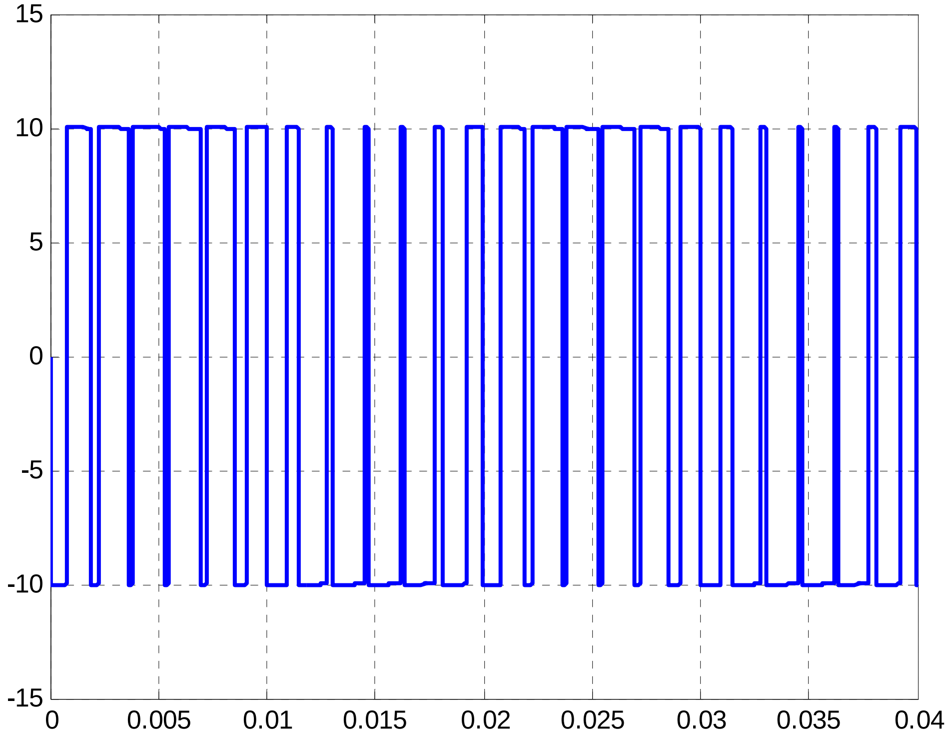


Fig 4.14 Bipolar PWM Output voltage waveform (single phase)

4.2.4 Pulse width modulation with Unipolar voltage switching [14]

In pulse width modulation with unipolar voltage switching, the switches in the two legs of the H-bridge in fig 4.10 are not switched simultaneously as in the previous bipolar scheme. Here, a carrier signal, v_{tri} triangle waveform is compares with two sinusoidal control signals shown in fig 4.15(a). The legs A and B of the full-bridge inverter are controlled by comparing v_{tri} with $v_{control}$ and $-v_{control}$, respectively. As shown in fig 4.15(a), the comparison of $v_{control}$ with the triangle waveform results in the following logic signals to control the switches in leg A:

$v_{control} > v_{tri}$: SW1 is on and $V_{AN}=V_d$.
$v_{control} < v_{tri}$: SW3 is on and $V_{AN}=0$.

The output voltage of inverter leg A with respect to the negative dc bus N is shown in fig 4.15(b). For controlling the leg B switches, $-v_{control}$ is compared with the same triangular waveform results in the following logic signals to control the switches in leg B:

$-v_{control} > v_{tri}$: SW2 is on and $V_{BN}=V_d$.
$-v_{control} < v_{tri}$: SW4 is on and $V_{BN}=0$.

The waveform of fig 4.15(d) shows that there are four combinations of switch on states and the corresponding voltage levels:

1. SW1 & SW4 ON: $V_{AN} = V_d$, $V_{BN} = 0$; $V_{AB} = V_d$.
2. SW3 & SW2 ON: $V_{AN} = 0$, $V_{BN} = V_d$; $V_{AB} = -V_d$.
3. SW1 & SW2 ON: $V_{AN} = V_d$, $V_{BN} = V_d$; $V_{AB} = 0$.
4. SW3 & SW4 ON: $V_{AN} = 0$, $V_{BN} = 0$; $V_{AB} = 0$.

When the both upper switches are on, the output voltage is 0v. The output voltage circulates in a loop through SW1 and SW2's diode or SW1's diode and SW2 depending on the direction of the output current. During this interval, the input current is zero. A similar condition occurs when both bottom switches SW3 and SW4 are on.

In this type of unipolar sinusoidal pulse width modulation scheme, when a switching occurs, the output voltage changes between zero and $+V_d$ or between zero and $-V_d$ voltage levels. That is why this type of PWM scheme is called unipolar sinusoidal pulse width modulation. This is opposed to the previous discussion, bipolar sinusoidal pulse width modulation which the voltage changes between $+V_d$ and $-V_d$.

This scheme has the advantage of “effectively” doubling the switching frequency as far as the output harmonics are concerned. The voltage jumps in the output voltage at each switching are reduced to V_d, as compared to bipolar scheme which is $2V_d$.

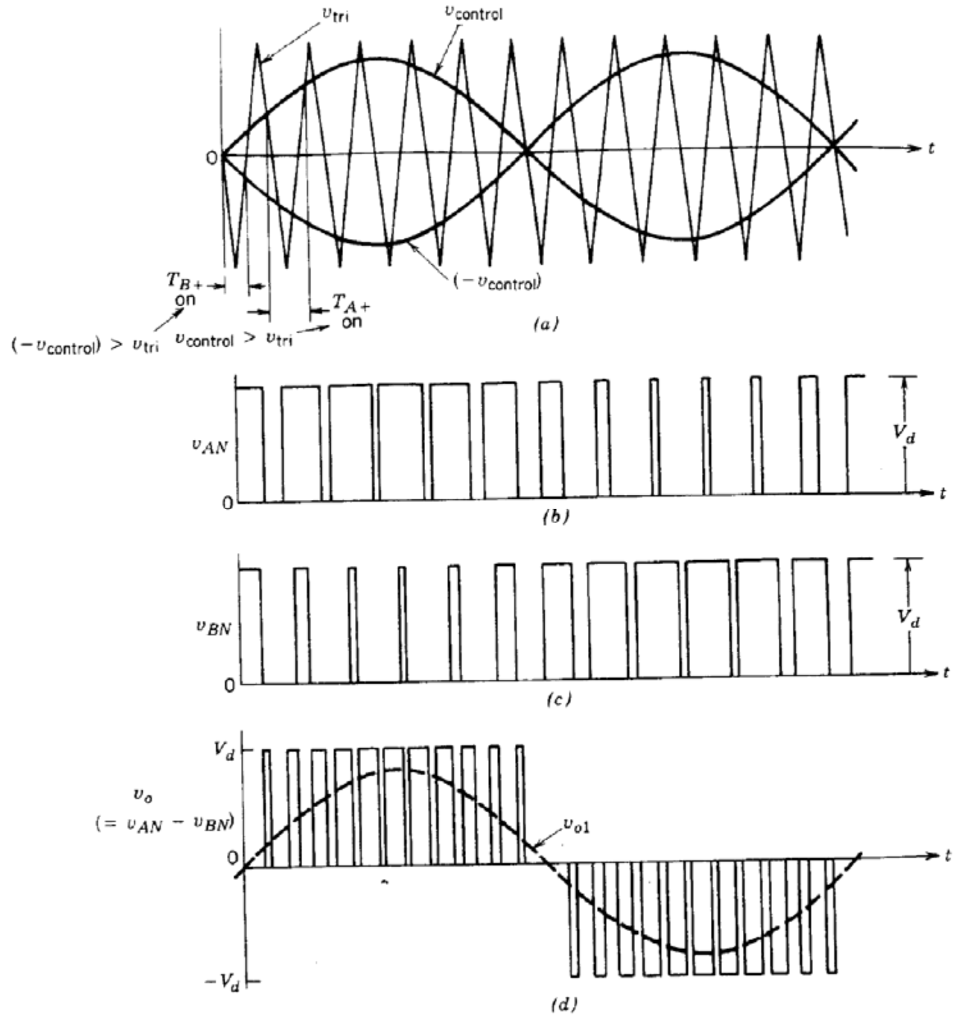


Fig 4.15 Unipolar Sinusoidal Pulse Width modulation

4.2.5 **Simulation study on Unipolar sinusoidal Pulse width modulation with MATLAB**

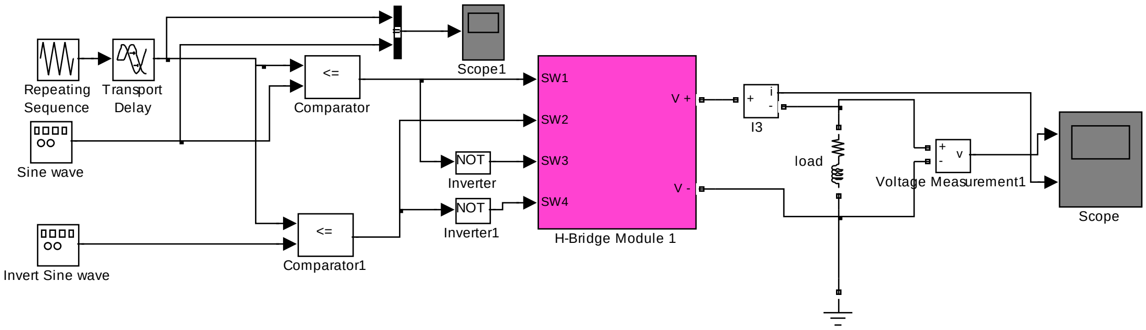


Fig 4.16 Unipolar switching in single phase H-bridge module

In fig 4.11, an Unipolar pulse width modulation single phase H-bridge with $\mathbf{m_a}$ =0.8 & $\mathbf{m_f}$ =12 is developed using MATLAB.

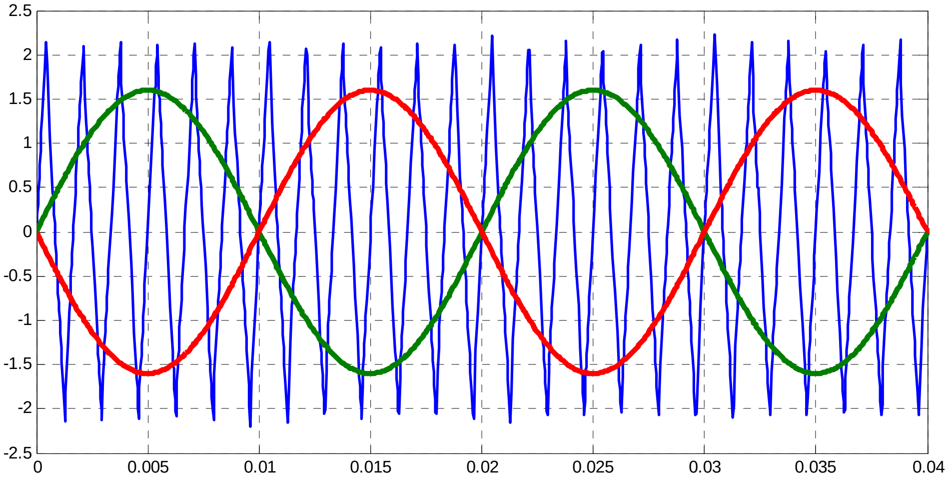


Fig 4.17 V_{control} & - V_{control} with a triangular signal (carrier) V_{tri}

In Fig 4.17, two control signals V_{control} and -V_{control} with amplitude 1.6V & frequency of 50Hz is compared with a carrier signal, V_{tri} triangle waveform with amplitude 2V & frequency of 600Hz. From the equation given in sub-section 4.2.1, $\mathbf{m_a}$ is calculated as 0.8 & $\mathbf{m}_f$ is calculated as 12.

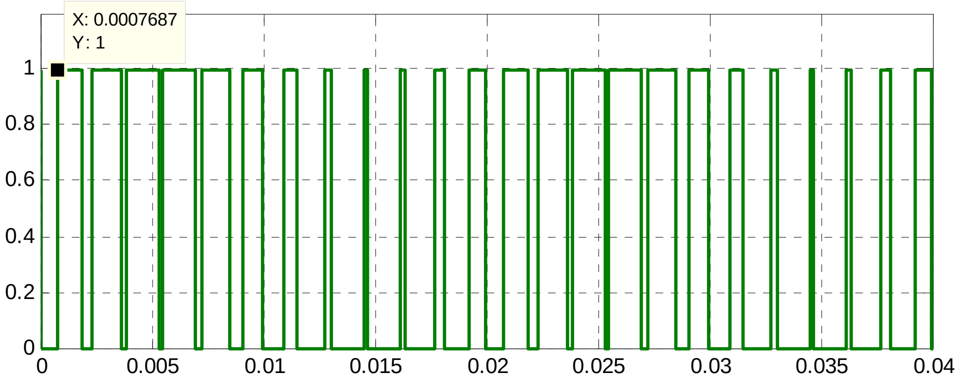


Fig 4.18 Gating signal from the top comparator output

As shown in fig 4.18, a signal is generated out from the top comparator (see fig 4.16) after the triangle waveform is compared with the control signal $V_{control}$ (sine wave).

When $V_{control} > V_{tri}$, gating signal is 'ON'. This gating signal is applied to SW1 and the inverted signal is applied to SW3.

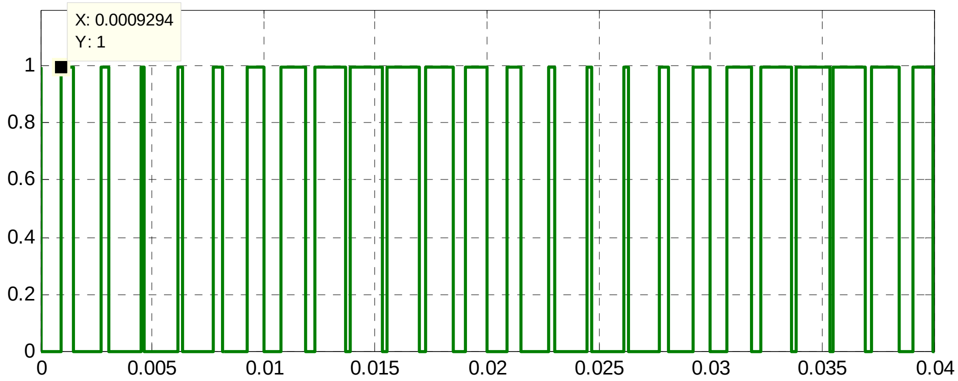


Fig 4.19 Gating signal from the bottom comparator output

As shown in fig 4.19, a signal is generated out from the bottom comparator (see fig 4.16) after the triangle waveform is compared with the control signal $-V_{control}$ (Inverted sine wave).

When -$v_{control}$ > v_{tri} , gating signal is 'ON'. This gating signal is applied to SW2 and the inverted signal is applied to SW4.

This technique produced three types of output voltage level. As shown in fig 4.20, the output voltage is +V_{dc} when SW1 & SW4 are turn on, and –V_{dc} when SW2 & SW3 are turn on, and zero when (SW1 & Sw2) or (SW3 & SW4) are turn on.

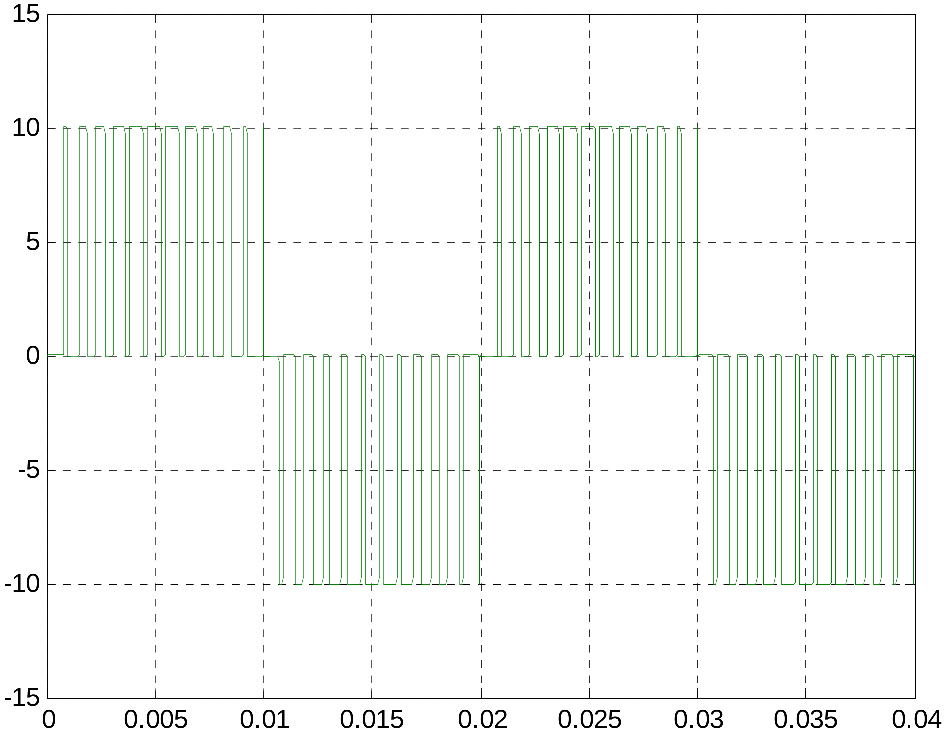


Fig 4.20 Unipolar PWM Output voltage waveform (single phase)

4.2.6 Simulation study on Improved type Unipolar sinusoidal Pulse width modulation with MATLAB [17]

An improvement has been made to the unipolar sinusoidal Pulse width modulation. Two triangular waveforms (carrier signal) are used instead of two control signals. The new improvement made used of one $V_{control}$ (sine wave) signal and compared with two triangular waveforms, V_{tri1} & V_{tri2}. V_{tri1} remained the same phase as mentioned above but the second triangular waveform, V_{tri2} is phase shift by 180°.

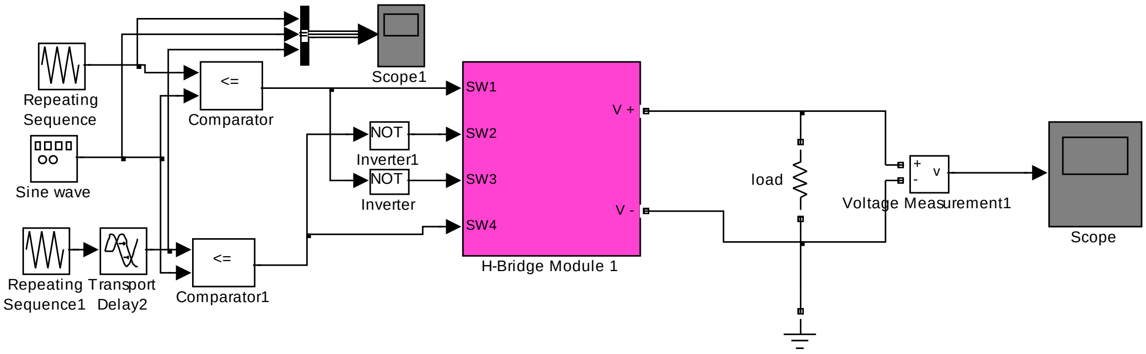


Fig 4.21 Improved Unipolar Pulse width modulation H-bridge module

In fig 4.21, an Improved Unipolar pulse width modulation single phase H-bridge with $\mathbf{m_a}$ =0.8 & $\mathbf{m_f}$ =12 is developed using MATLAB.

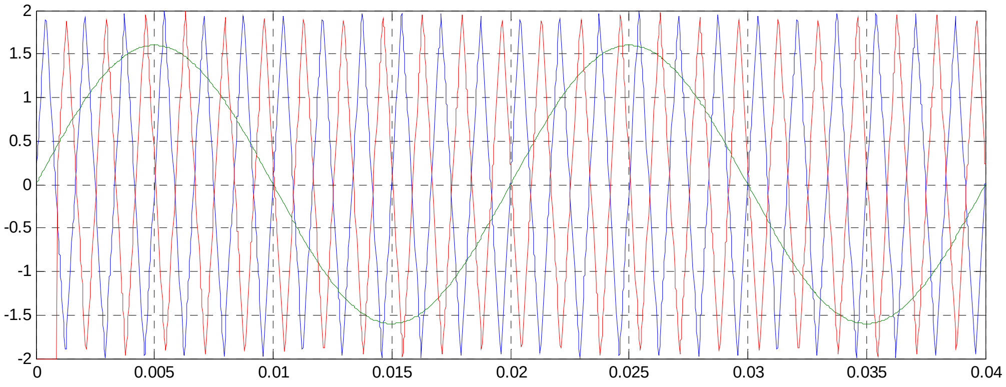


Fig 4.22 $V_{control}$ with two triangular signals (carrier) V_{tri1} & V_{tri2}

In Fig 4.22, one control signal $V_{control}$ with amplitude 1.6V & frequency of 50Hz is compared with two carrier signal, $V_{tri\ 1}$ and $V_{tri\ 2}$ triangle waveforms with amplitude 2V & frequency of 600Hz. $V_{tri\ 2}$ is 180° phase shift from $V_{tri\ 1}$.

The gating signal is generated out from the top comparator (see fig 4.21) after the triangle waveform $v_{tri\ 1}$ is compared with the control signal $v_{control}$ (sine wave).

When $v_{control} > v_{tri1}$, gating signal is 'ON'. This gating signal is applied to SW1 and the inverted signal is applied to SW3.

The gating signal is generated out from the bottom comparator (see fig 4.21) after the triangle waveform $v_{tri\ 2}$ is compared with the control signal $v_{control}$ (sine wave).

When $v_{control} > v_{tri2}$, gating signal is 'ON'. This gating signal is applied to SW4 and the inverted signal is applied to SW2.

This technique produced three types of output voltage level. As shown in fig 4.23, the output voltage is $+V_{dc}$ when SW1 & SW4 are turn on, and $-V_{dc}$ when SW2 & SW3 are turn on, and zero when (SW1 & Sw2) or (SW3 & SW4) are turn on. This is similar to unipolar PWM voltage switching scheme.

For this improved type of unipolar PWM voltage switching, the advantage will be discussed further in the later section where PI controller is implemented.

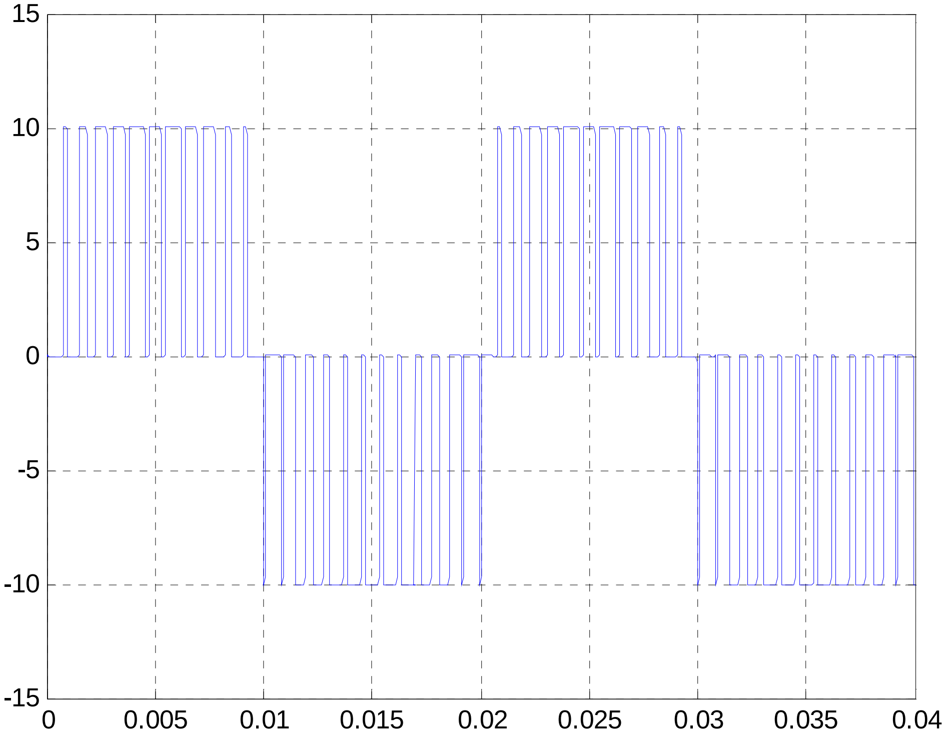


Fig 4.23 Improved Unipolar PWM Output voltage waveform (single phase)

4.2.7 Square-wave modulation

Square wave modulation is also a form of sinusoidal pulse width modulation, where $\mathbf{m_a}$ becomes so large that the output voltage becomes square wave. The sinusoidal control voltage waveform intersects with the triangular waveform only at zero crossing of $V_{control}$. Therefore, the switching devices are switched with a duty cycle of 0.5 (180°) of the desired output frequency and the output voltage is independently of $\mathbf{m_a}$**.**

This technique of switching is similar to method discussed in section 4.1 except that the gating signal is generated by comparing a sinusoidal waveform and triangular waveform.

One of the serious disadvantages of square-wave modulation is that the inverter is not capable of regulating the output voltage magnitude. Thus, the dc input V_d to the inverter must be adjusted in order to control the magnitude of the inverter output voltage.

4.2.8 Simulation study on Square wave sinusoidal Pulse width modulation with MATLAB

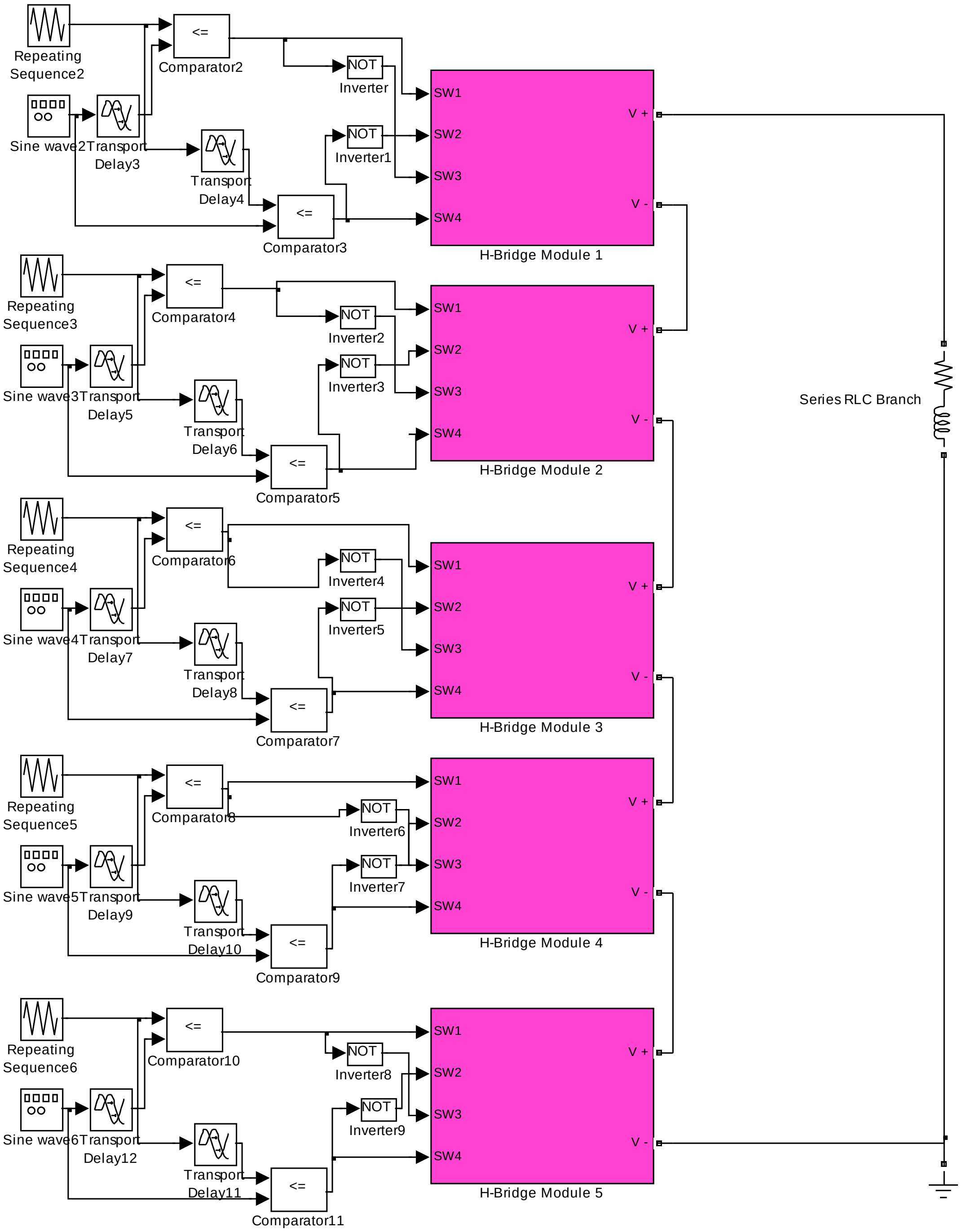


Fig 4.24 Square wave Pulse width modulation for 11-level multilevel inverter

In fig 4.24, a square wave pulse width modulation single phase 11 level multilevel H-bridge inverter $\mathbf{m_a} > 1.0$ is developed using MATLAB.

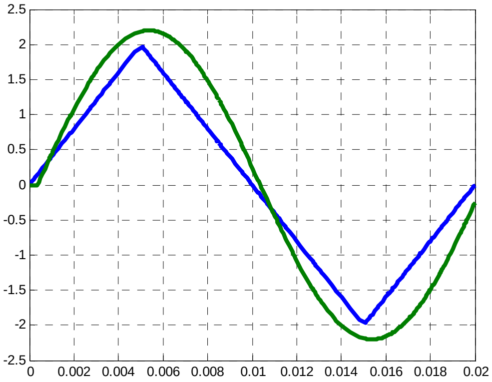


Fig 4.25 V_{control} with triangular signal (carrier) V_{tri}

As shown in fig 4.25, the sinusoidal wave amplitude is above the triangular waveform amplitude ($\mathbf{m_a} > 1.0$).

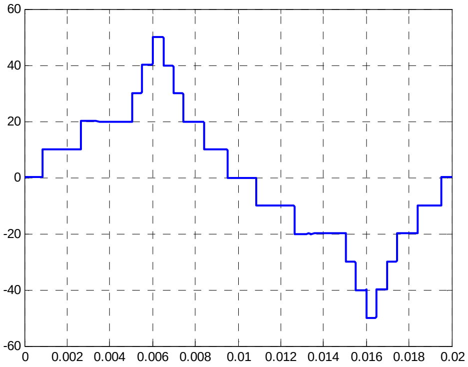


Fig 4.26 Output voltage waveform of 11 level multilevel inverter

As shown in fig 4.26, the output voltage waveform is similar to the one discussed in section 4.1 ($\mathbf{m_a} > 1.0$).

5. Control Technique used for the multilevel inverter [16]

5.1 Shift Pulse width modulation technique

This technique uses a number of wave carriers equal to the number of full bridge inverters employed in the cascaded inverter structure. The phase shift on the subsequent carrier waveforms is shifted by $1/(m \times f_{tri})$, where m is the number of H-bridge module and f_{tri} is the frequency of the carrier waveform. For example, for 11 level inverter topology, there are 5 numbers of H-bridge modules used. Thus, the wave carrier is phase shifted by $1/(5 \times f_{tri})$.

An example on the control strategy is illustrated below.

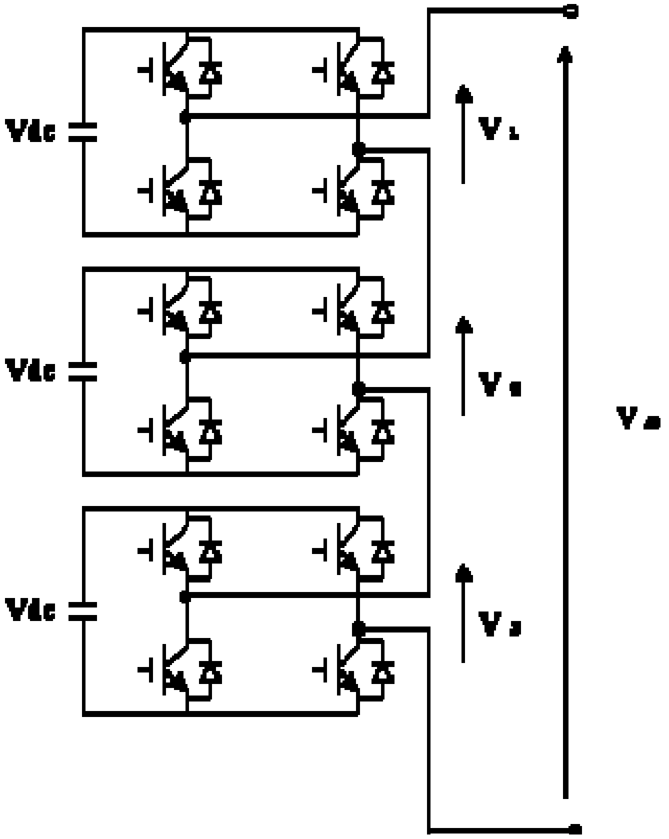


Fig 5.1 7-level cascaded multilevel inverter

Some terms are needed to be defined in the following illustration.

- $i = 1 \ldots 3$ (number of full bridge inverters) employed for 7 level cascaded inverter.
- S_{1i} and S_{2i} are the upper switch of each full bridge inverter.

In this Pulse Width Modulation technique, shift PWM techniques, the carriers signal (triangular waveform) are shifted by 1/(3 x f_{tri}), where f_{tri} is the frequency of the carrier reference waveform.

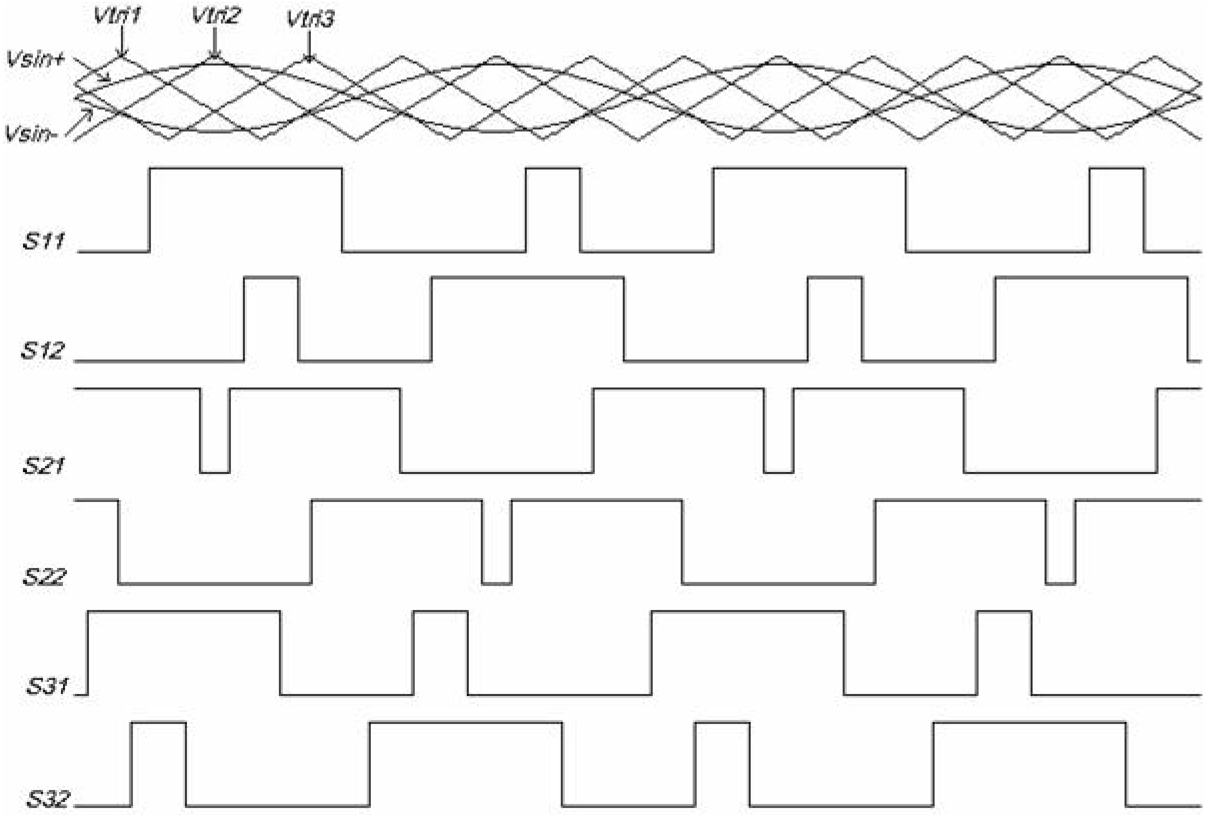


Fig 5.2 Shift PWM Technique for a 7 level cascaded inverter

In fig 5.2, it shows the shift PWM technique for 7 level cascaded inverter for $\mathbf{m_a} = 0.8$ and $\mathbf{m}_f = 2$.

Note that this technique used is corresponding to Unipolar voltage switching scheme, where two control signals is compared to a single carrier signal.

- S11 & S21 is applied to the 1st H-bridge module, SW1 & SW2. The inverted signal of S11 & S21 is applied to SW3 & SW4 respectively.
- S12 & S22 is applied to the 2nd H-bridge module, SW1 & SW2. The inverted signal of S12 & S22 is applied to SW3 & SW4 respectively.
- S31 & S32 is applied to the 3rd H-bridge module, SW1 & SW2. The inverted signal of S12 & S22 is applied to SW3 & SW4 respectively.

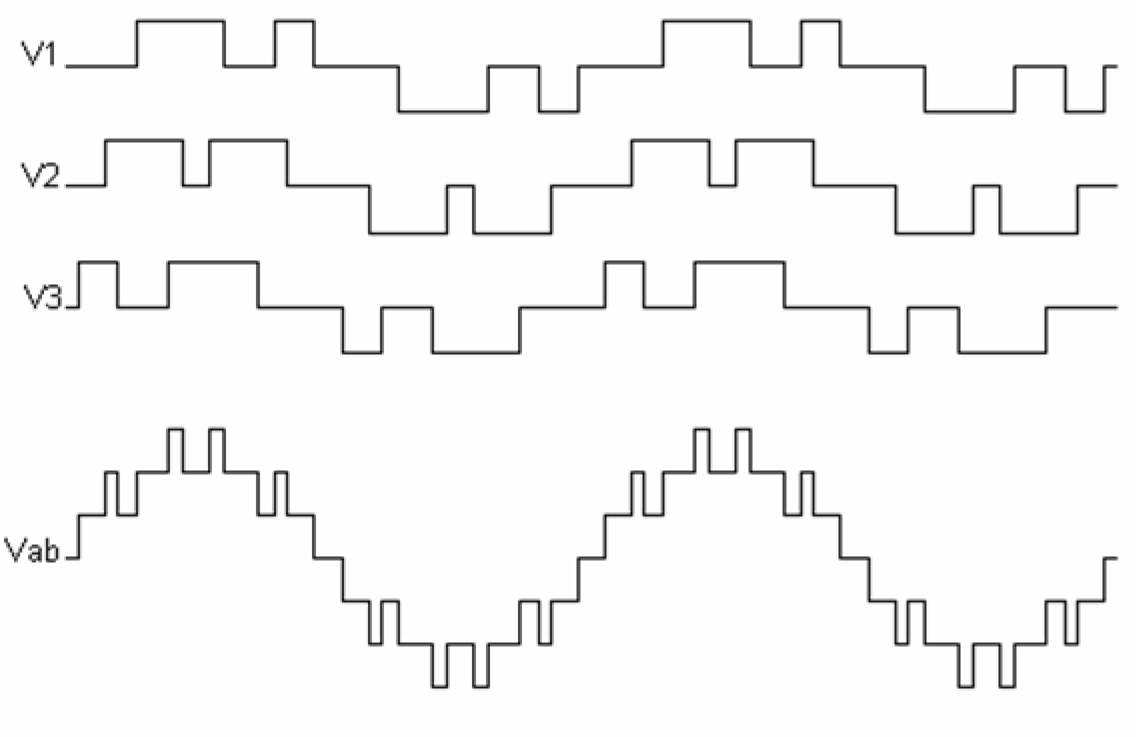


Fig 5.3 Output voltages of a 7 level single phase cascaded inverter

In fig 5.3, it shows the output voltage of each full bridge inverter and the output voltage of the multilevel inverter for $\mathbf{m_a}$ = 0.8 and $\mathbf{m}_f$ = 2.

5.2 Simulation study on shift pulse width modulation technique With MATLAB

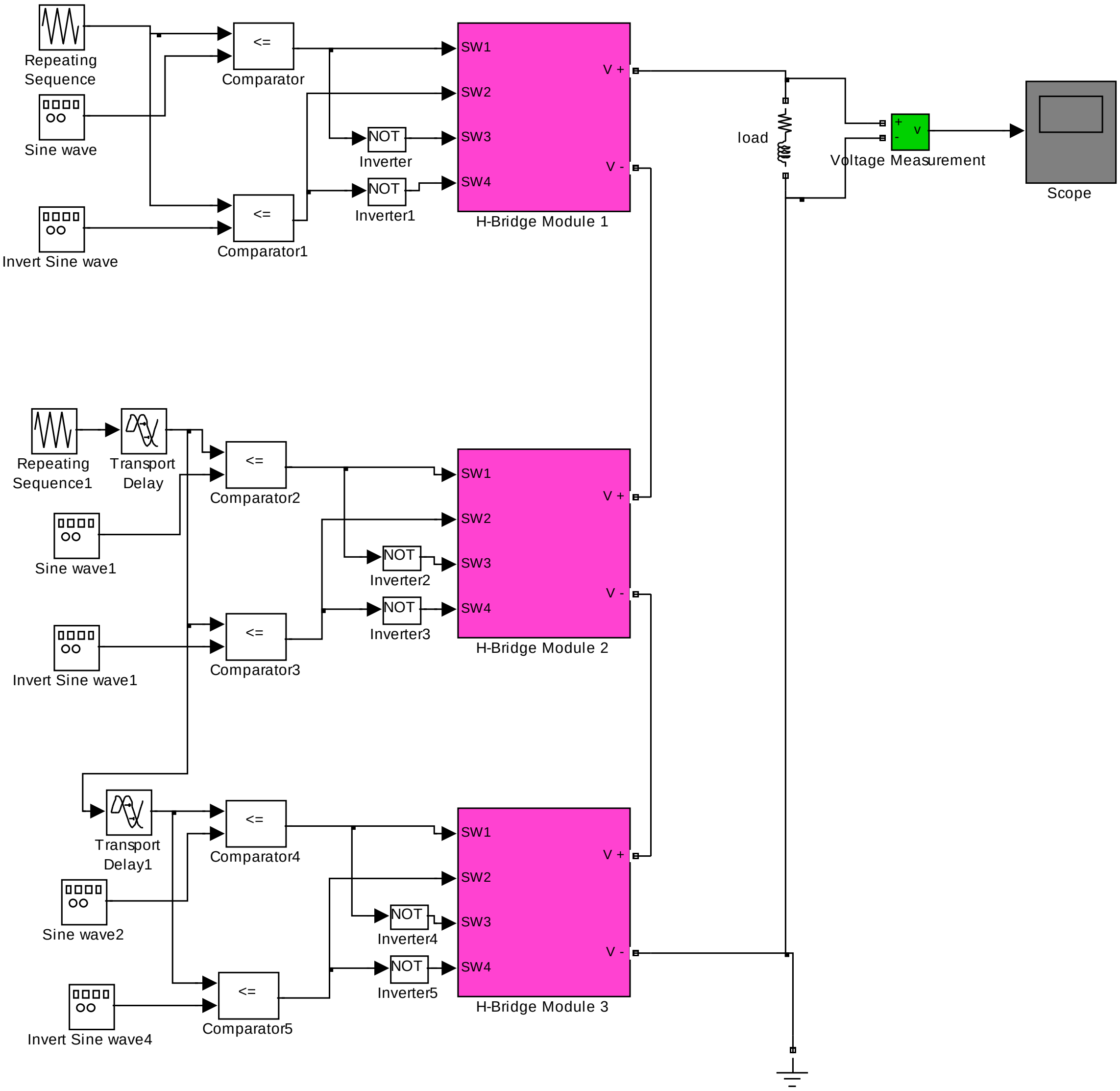
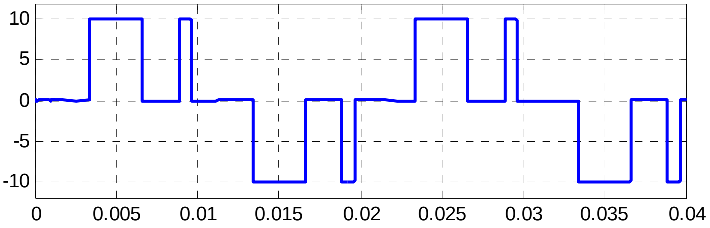
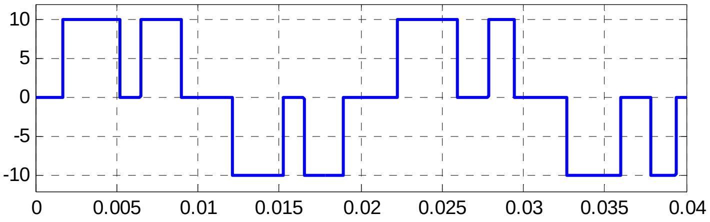


Fig 5.4 Shift technique Pulse width modulation for 7-level multilevel inverter

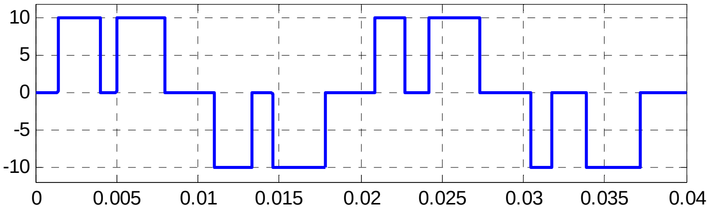
In fig 5.4, a shift technique pulse width modulation single phase 7 level multilevel H-bridge inverter $\mathbf{m_a} = 0.8$ & $\mathbf{m}_f = 2$ is developed using MATLAB. This is to verify the modeling study of pulse width modulation control technique as discussed in section 5.1.



(a) V1-first full bridge output voltage waveform



(b) V2-second full bridge output voltage waveform



(c) V3-third full bridge output voltage waveform

Fig 5.5 Output voltage of each full bridge inverter for 7 level multilevel inverter

This simulation uses 3 numbers of wave carriers & 3 set of sine wave & inverted sine wave, $V_{control}$ & $-V_{control}$. The phase shift on the subsequent carrier waveforms is shifted by $1/(3 \times f_{tri})$, where f_{tri} is the frequency of the carrier waveform, 100Hz.

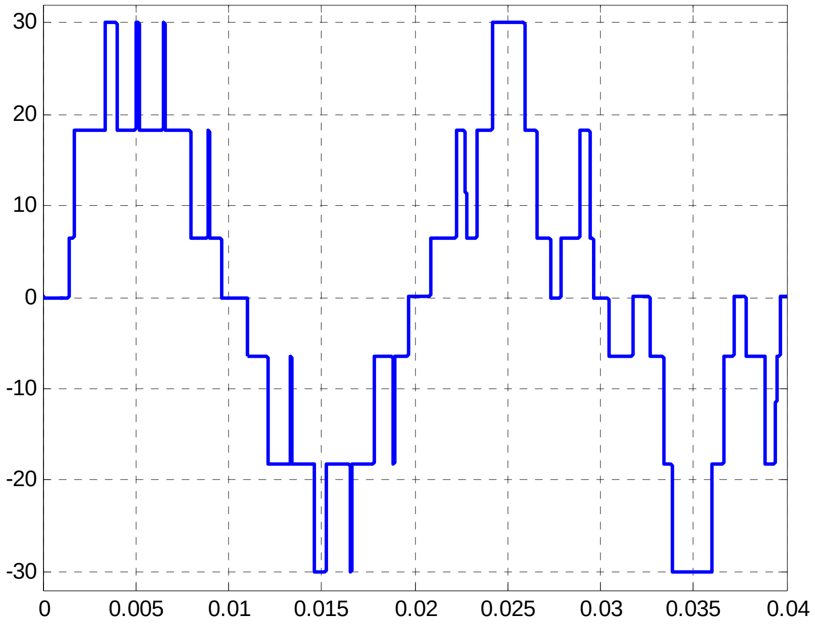


Fig 5.6 Output voltage waveform of 7 level single phase multilevel inverter

In fig 5.6, the output voltage waveform shows a bit different from the modeling study as discussed in section 5.1. This is due to the different in the starting point of the carrier frequencies from the modeling study and the simulation study in MATLAB.

5.3 Discussion on the selection of switching frequency [14]

The selection of the switching frequency and the frequency modulation ratio $\mathbf{m}_f$ shall be discuss in this section. The filtering of harmonic voltage is easy at high frequencies, thus it is desirable to use as high a switching frequency as possible. There is one significant drawback which is switching losses in the inverter switches increase proportionally with the switching frequency f_{tri}.

In most applications, the switching frequency is selected to be either less than 6 KHz or greater than 20 KHz. In 50 Hz or 60 Hz type applications, such as ac motor drives, where the fundamental frequency of the inverter output may be required to be as high as 200 Hz, the frequency modulation ratio $\mathbf{m}_f$ maybe 9 or less for switching frequency of less than 2 KHz. For switching frequencies higher than 20 KHz, $\mathbf{m}_f$ will be larger than 100. $\mathbf{m}_f$ = 21 is treated as the borderline between large and small.

For small $\mathbf{m}_f$ ($\mathbf{m}_f \leq 21$) – Synchronous PWM. For small value of $\mathbf{m}_f$, the triangular waveform signal V_{tri} and the control signal V_{control} should be synchronized to each other. The Synchronous PWM requires that $\mathbf{m}_f$ to be an integer. This means that the triangular waveform frequency can be varies with the desired inverter frequency. For example, if the inverter output frequency is 50 Hz and $\mathbf{m}_f = 21$, the triangular waveform frequency V_{tri} must be 50 Hz X 21 = 1050 Hz. The reason for using synchronous PWM is that the asynchronous PWM results in subharmonics that are very undesirable in most applications.

For large $\mathbf{m}_f$ ($\mathbf{m}_f > 21$) – Here, at large values of $\mathbf{m}_f$, the amplitudes of subharmonics due to asynchronous PWM are small. Thus, at large value of $\mathbf{m}_f$, the asynchronous PWM can be used where the frequency of the triangular waveform is kept constant and the frequency of control signal V_{control} varies which results in non-integer values of $\mathbf{m}_f$. If the load is ac motor, the subharmonics at zero or low frequency will results in large currents that are undesirable even the subharmonics amplitude is small. Thus, asynchronous PWM must be avoided.

Next section will be the simulation studies on various $\mathbf{m}_f$ values and level (depend on numbers of H-bridge module used).

5.4 Simulation study on Unipolar PWM multilevel inverter With MATLAB

7-level multilevel inverter with $\mathbf{m_a}$ =1.0, $\mathbf{m}_f$=12

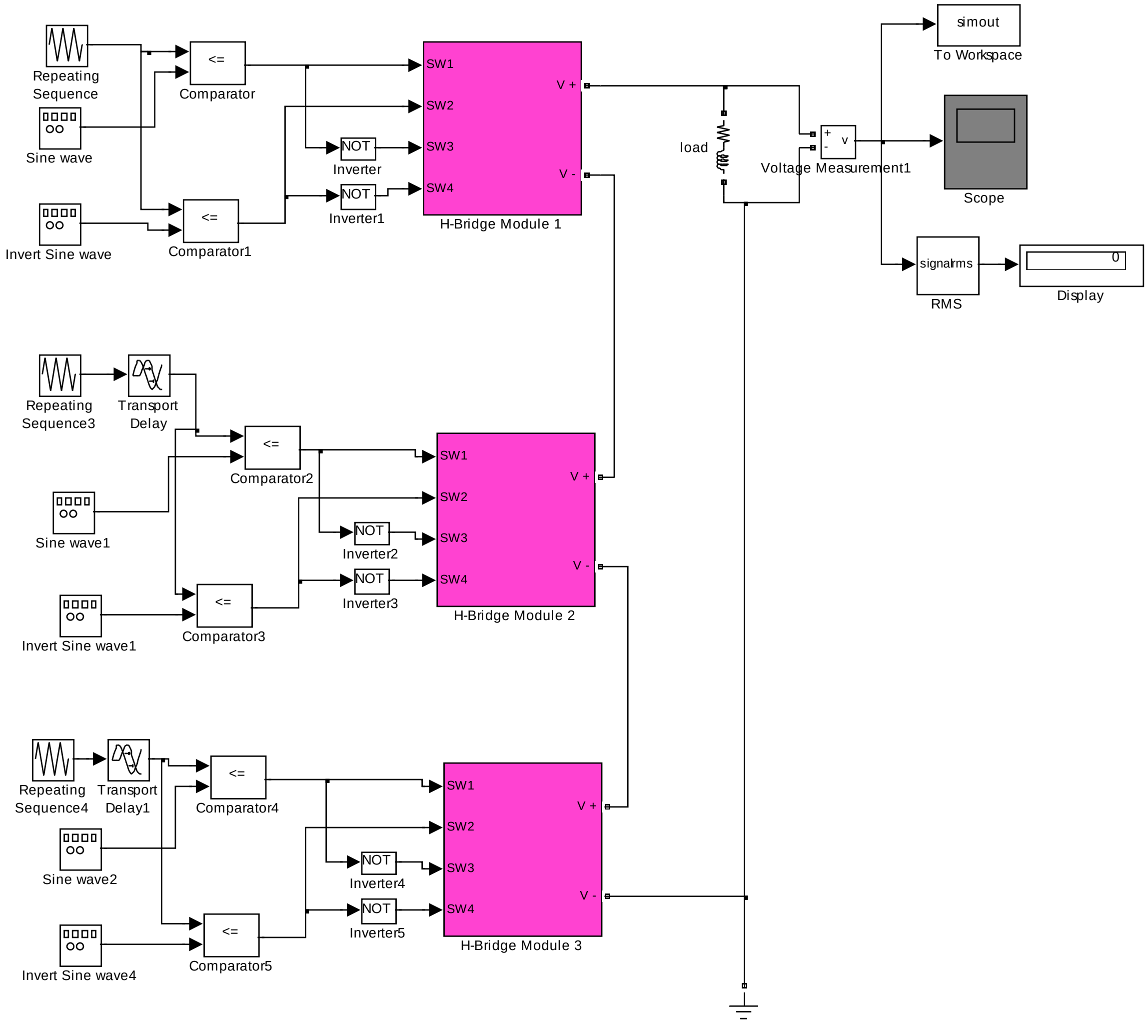


Fig 5.7 Unipolar PWM multilevel inverter

In fig 5.7, it shows a 7-level multilevel inverter model with $\mathbf{m_a}$ =1.0, $\mathbf{m}_f$=12 built in MATLAB. The output waveform is shown in fig 5.8. The RMS value calculated is 22.43V. Simulation studies on subsequent decreasing value of $\mathbf{m_a}$ are carried out in the next sub-sections.

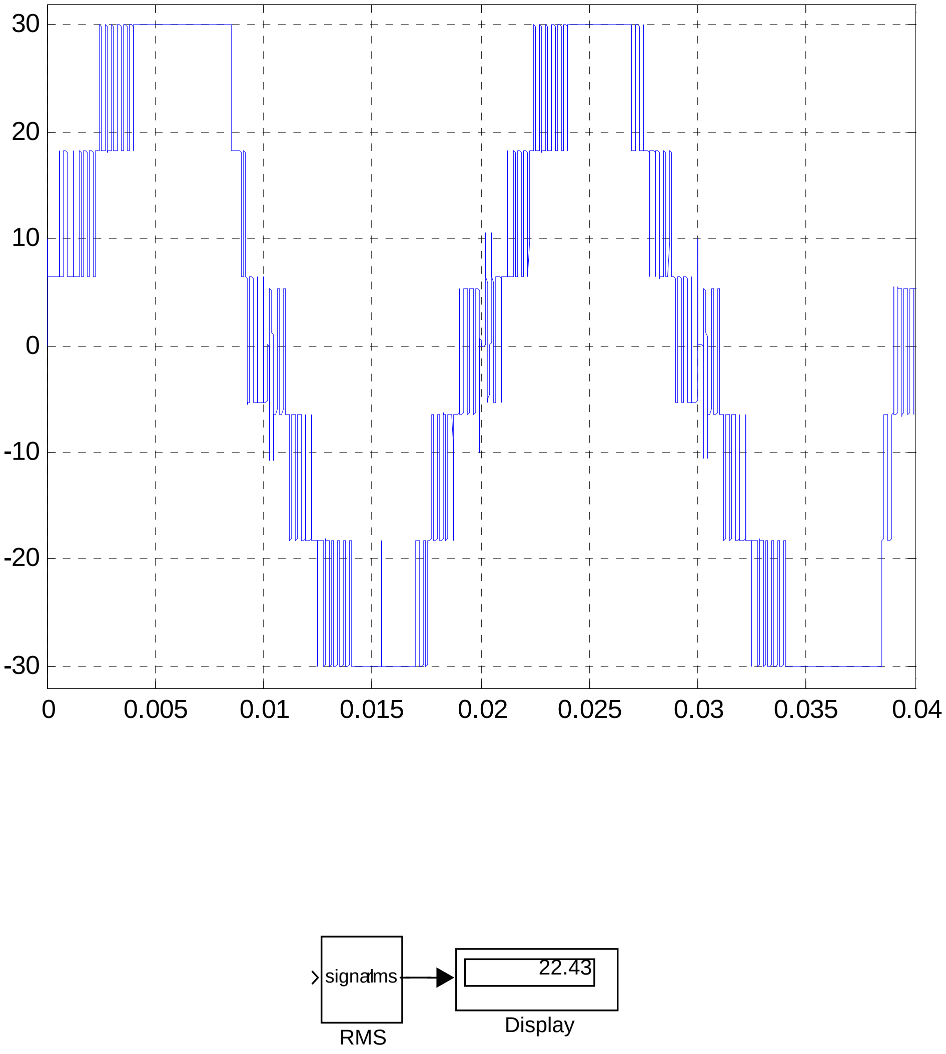


Fig 5.8 Output voltage waveform and RMS value

7-level multilevel inverter with $\mathbf{m}_a$ =0.9, $\mathbf{m}_f$ =12

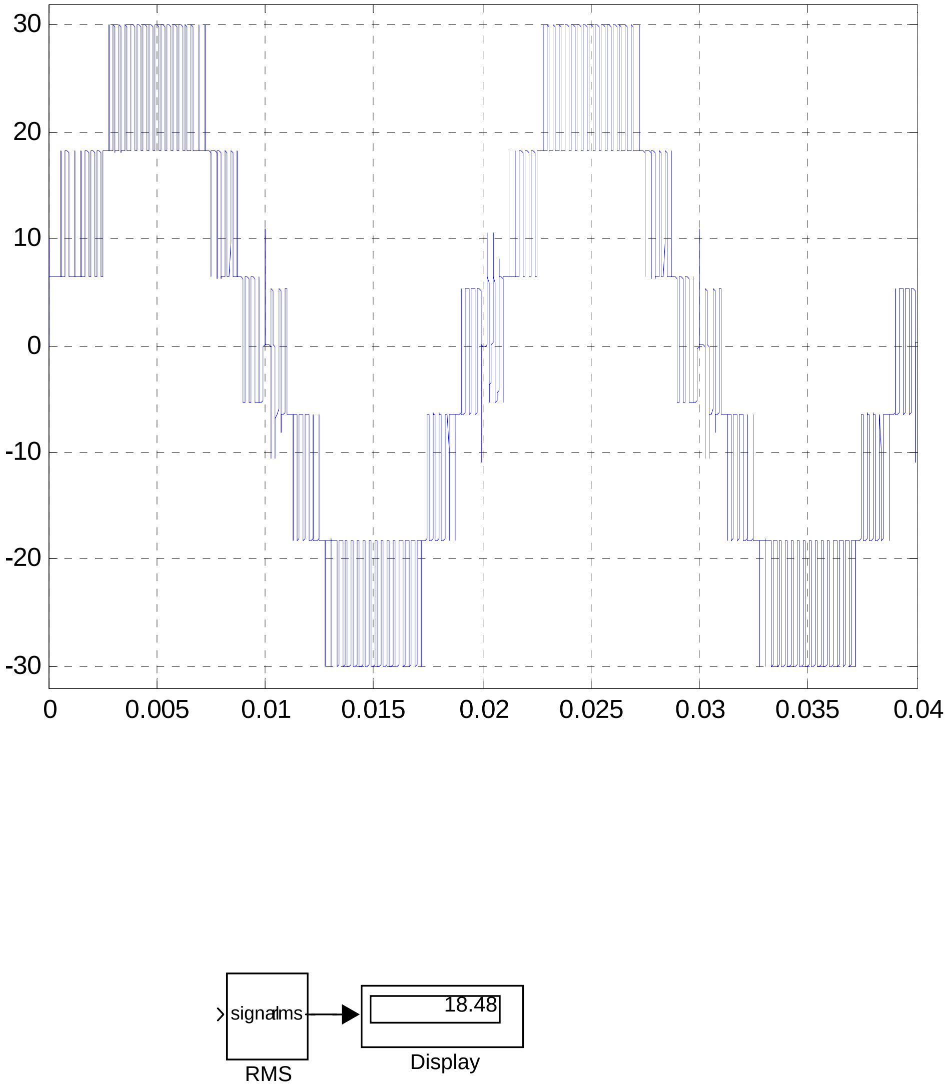
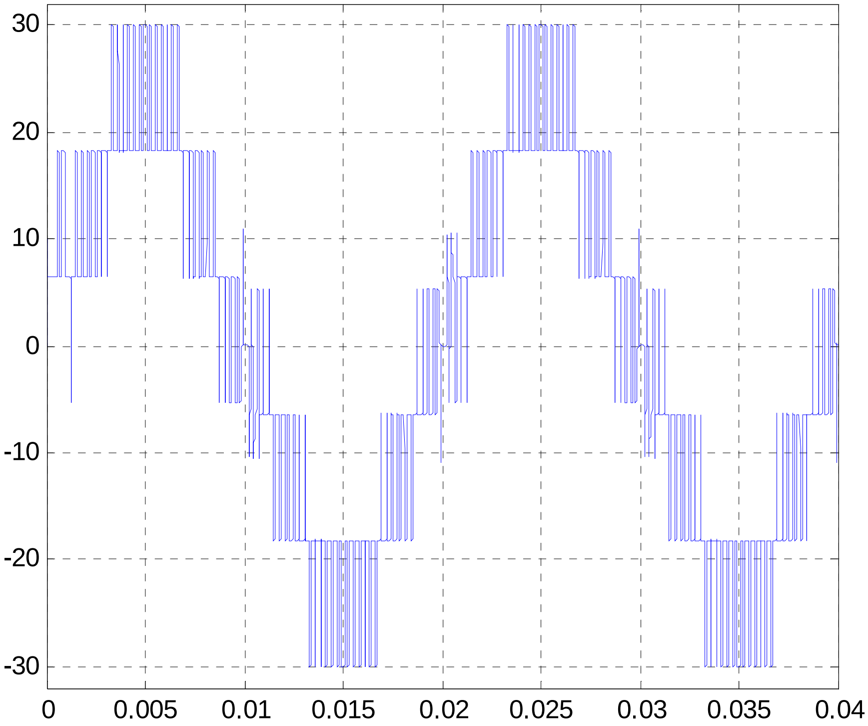


Fig 5.9 Output voltage waveform and RMS value

The output voltage waveform of 7-level PWM multilevel inverter with $\mathbf{m}_a$ =0.9, $\mathbf{m}_f$ =12 is shown in Fig 5.9. The RMS value is calculated as 18.48V.

7-level multilevel inverter with $\mathbf{m_a}$ =0.8, $\mathbf{m}_f$ =12



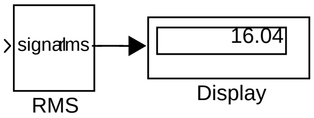


Fig 5.10 Output voltage waveform and RMS value

The output voltage waveform of 7-level PWM multilevel inverter with $\mathbf{m_a}$ =0.8, $\mathbf{m}_f$ =12 is shown in Fig 5.10. The RMS value is calculated as 16.04V. Subsequent simulation on different $\mathbf{m_a}$ is carried out and compile in table format.

m_a	1.0	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1	0.0
RMS value	22.43	18.48	16.04	13.54	11.46	9.29	6.93	5.53	5.02	3.67	0.0

Table 5.1 Voltage output Vs $\mathbf{m_a}$

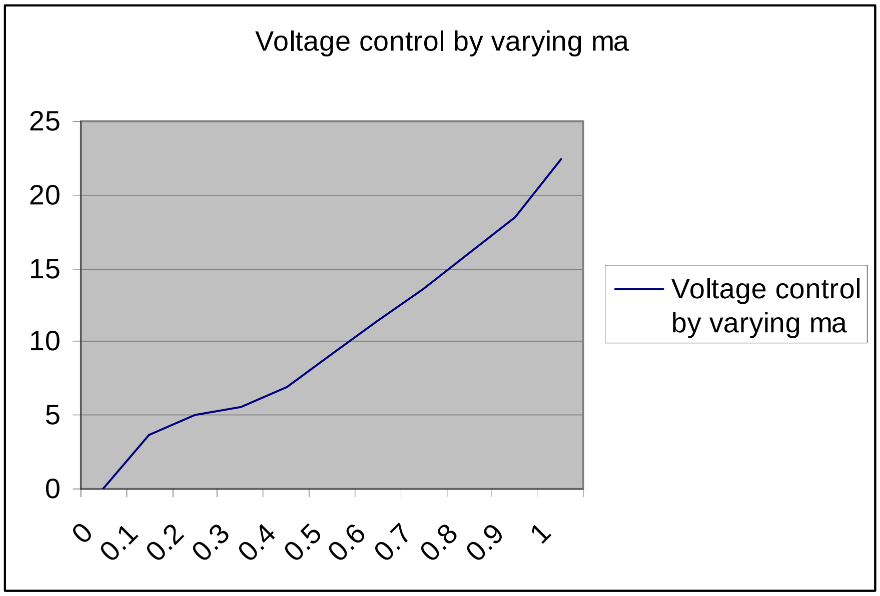


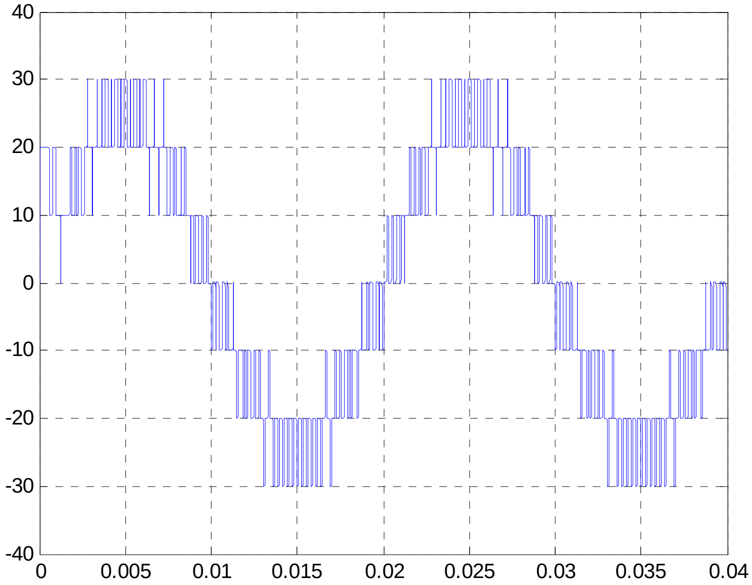
Fig 5.11 Voltage output Vs $\mathbf{m_a}$

As explained in section 4.2.1, the amplitude modulation ratio controls the amplitude of the fundamental frequency voltage in two regions. One region is $\mathbf{m_a \leq 1.0}$, the fundamental frequency voltage varies linearly with $\mathbf{m_a}$. Simulation studies on different values of $\mathbf{m_a}$ are carried out and tabulated in table 5.1. Chart is plotted base on the values tabulated as shown in fig 5.11. The chart show that the value plotted is almost linearly increases with $\mathbf{m_a}$.

6. Simulation study on different level used on the improved type unipolar PWM multilevel inverter with MATLAB.

As explained in sub-section 4.2.6, an improvement has been made to the unipolar sinusoidal Pulse width modulation. Two triangular waveforms (carrier signal) are used instead of two control signals. The new improvement made used of one $V_{control}$ (sine wave) signal and compared with two triangular waveforms, V_{tri1} & V_{tri2}. V_{tri1} remained the same phase but the second triangular waveform, V_{tri2} is phase shift by 180°. The simulation studies on different level used improved type unipolar PWM multilevel inverter with MATLAB is discuss as follow. This method will minimize the complexity when a PI controller is implemented so that the controller will only need to regulate one control signal $V_{control}$ instead of two. The PI controller will be develop and explain in the next section.

6.1 7-level improved type Unipolar multilevel inverter



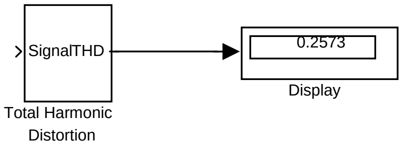
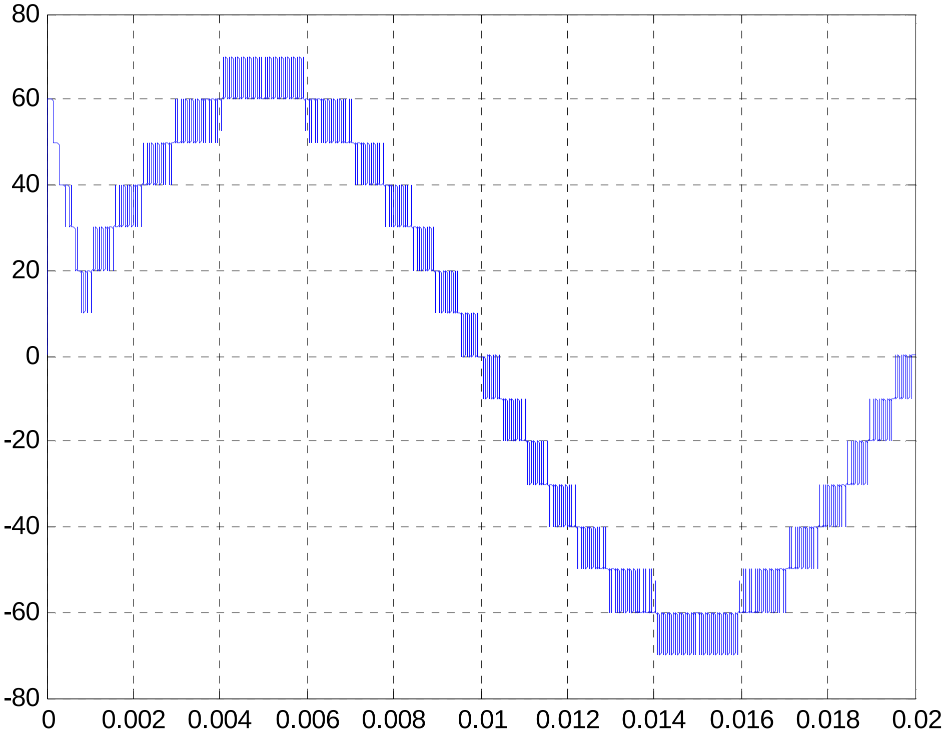


Fig 6.1 Output voltage waveform and THD for 7-level inverter

As shown in Fig 6.1, the output voltage waveform is shown for 7-level improved type unipolar PWM $\mathbf{m_a}$ =0.8, $\mathbf{m}_f$=12 multilevel inverter. The Total Harmonic Distortion is 25.73%.

6.2 15-level improved type Unipolar multilevel inverter



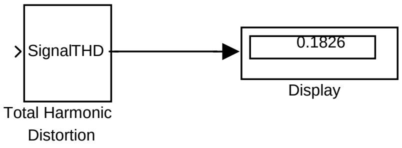
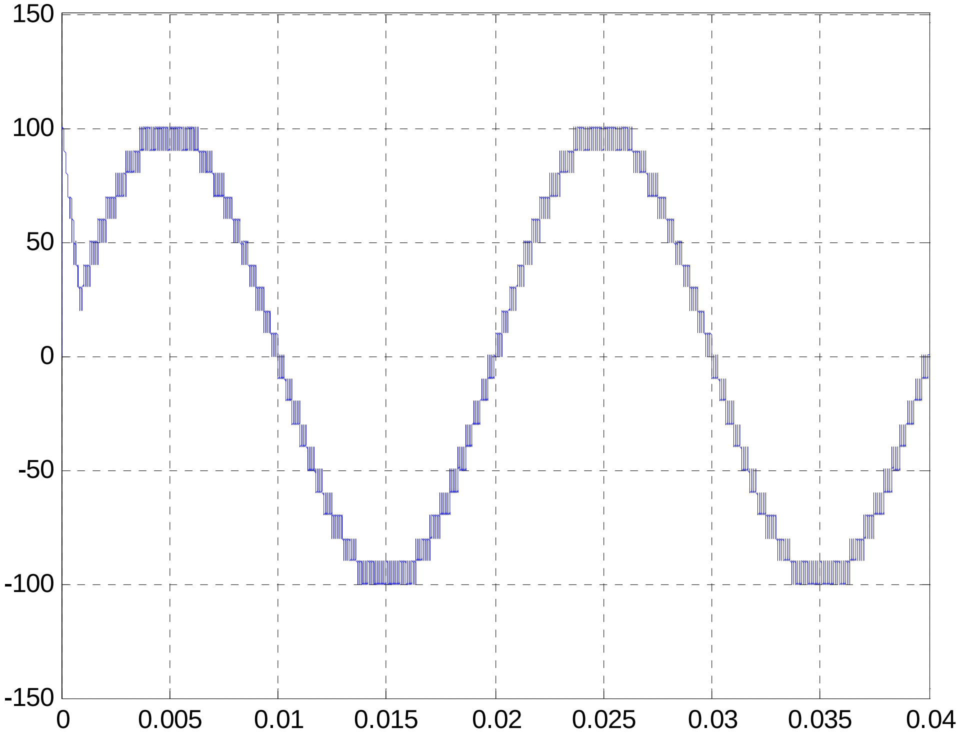


Fig 6.1 Output voltage waveform and THD for 15-level inverter

As shown in Fig 6.2, the output voltage waveform is shown for 15-level improved type unipolar PWM $\mathbf{m_a}$ =0.9, $\mathbf{m}_f$ =21 multilevel inverter. The Total Harmonic Distortion is 18.26%.

6.3 23-level improved type Unipolar multilevel inverter



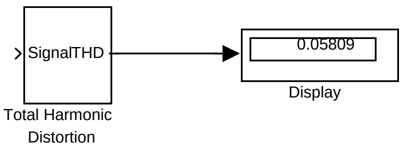


Fig 6.3 Output voltage waveform and THD for 23-level inverter

As shown in Fig 6.3, the output voltage waveform is shown for 23-level improved type unipolar PWM $\mathbf{m}_a$ =0.9, $\mathbf{m}_f$=21 multilevel inverter. The Total Harmonic Distortion is 5.80%.

It can be seen that as the number of levels increases, the synthesized output waveform has more steps, which produces a staircase wave that approaches a desired waveform. From the different simulation performed, as more steps are added to the waveform, the total harmonic distortion of the output waveform decreases, as the number of levels increase, the total output voltage by summing up multiple voltage levels also increases.

7. Proportional-Integral Controller

7.1 Introduction to PID controller [18]

The characteristic of proportional (P), integral (I) and derivative (D) controls in PID controller shall be discuss in this section.

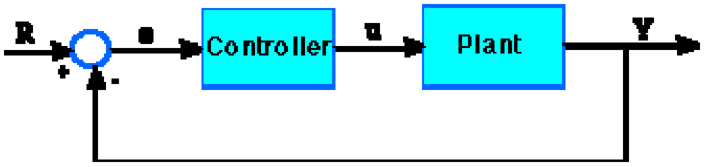


Fig 7.1 A feedback system

The transfer function of PID controller is:

$$K_p + \frac{K_I}{s} + K_d s = \frac{K_d s^2 + K_p s + K_I}{s}$$

where Kp = Proportional gain,
KI = Integral gain &
Kd = Derivative gain.

In fig 7.1, the variable (e) represents the error, where (e) = difference between the desired input value (R) and the actual output (Y). Error signal will be sent to the controller, the signal (u) is equal to the {proportional gain (Kp) X the magnitude of the error} + {integral gain (KI) X integral of the error} + {derivative gain (Kd) X derivative of the error}. The signal (u) will then sent to the plant, new output (Y) will be obtained. The process goes on and on.

7.2 Developing of PI controller using MATLAB

In this project, a PI controller will be develop to eliminate the need for manual adjustment of $V_{control}$ (sine wave) signal to compensate for the output voltage drop or gain during the variation of the load.

Proportional controller adjusts the output signal in direct proportional to the error signal. It will have the effect of reducing the error but does not eliminating the error. Thus, an Integral controller is required to eliminate any offset occur between the desired and actual value.

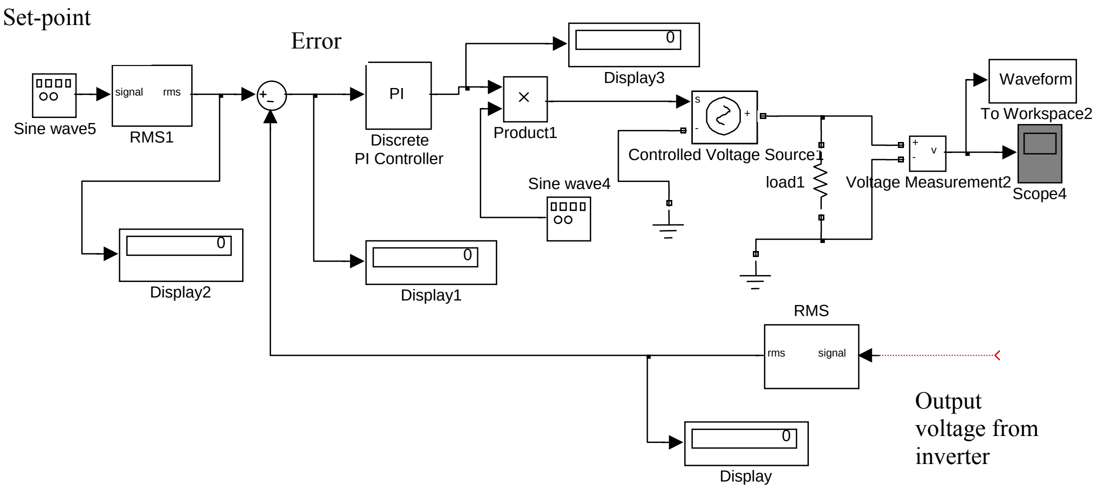


Fig 7.2 PI controller schematic in MATLAB

The simulation process here uses pulse width modulation and PI controller to control the RMS output voltage of the inverter. The improved type unipolar pulse width modulation is selected for this simulation due to its switch scheme which is the improvement of changing two control signals to one control signal for better integration with the PI controller. This greatly reduced the complexity in trying to control two signals at one time.

7.3 Simulation study on 7-level multilevel inverter with PI controller

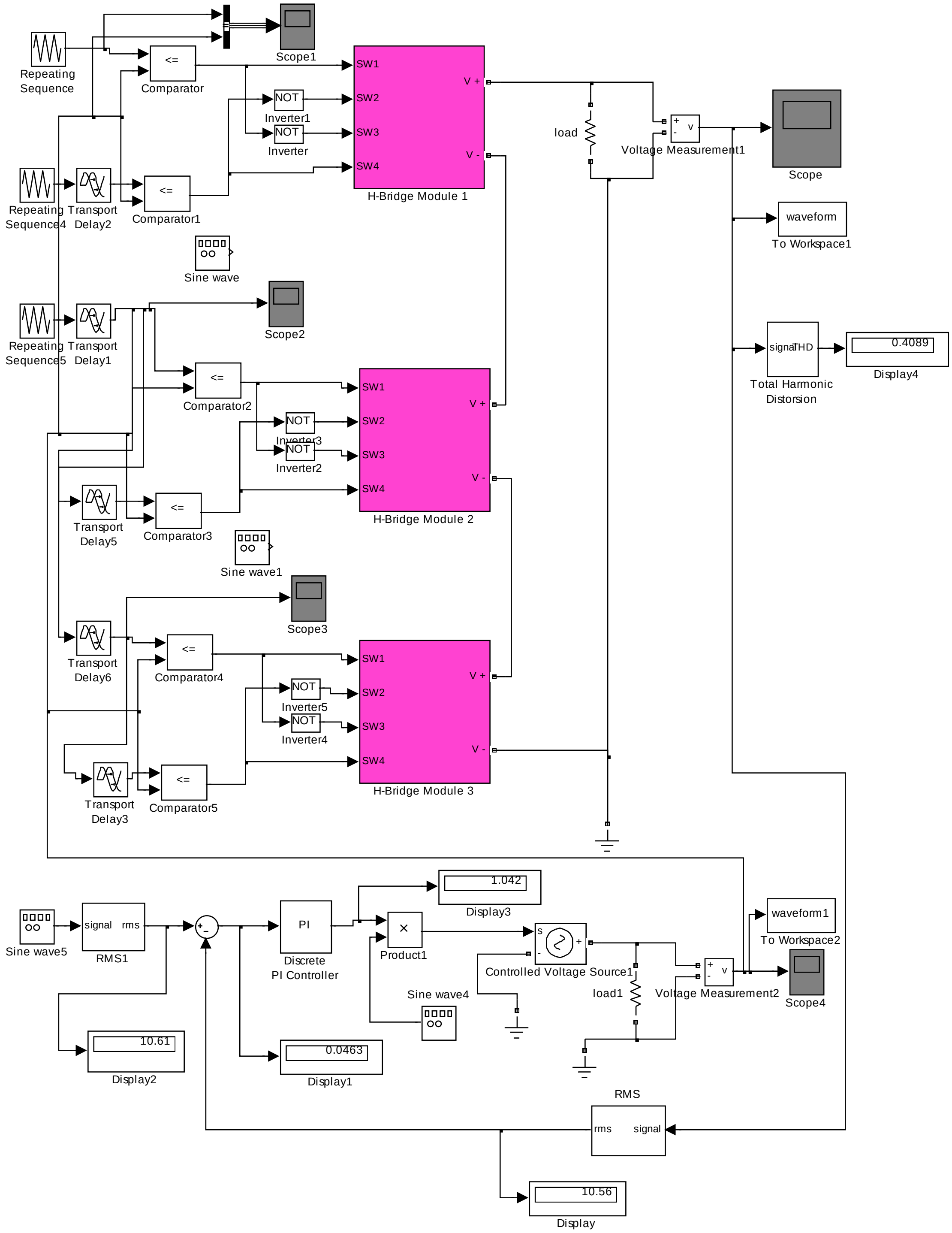


Fig 7.3 7-level inverter with PI controller model in MATLAB

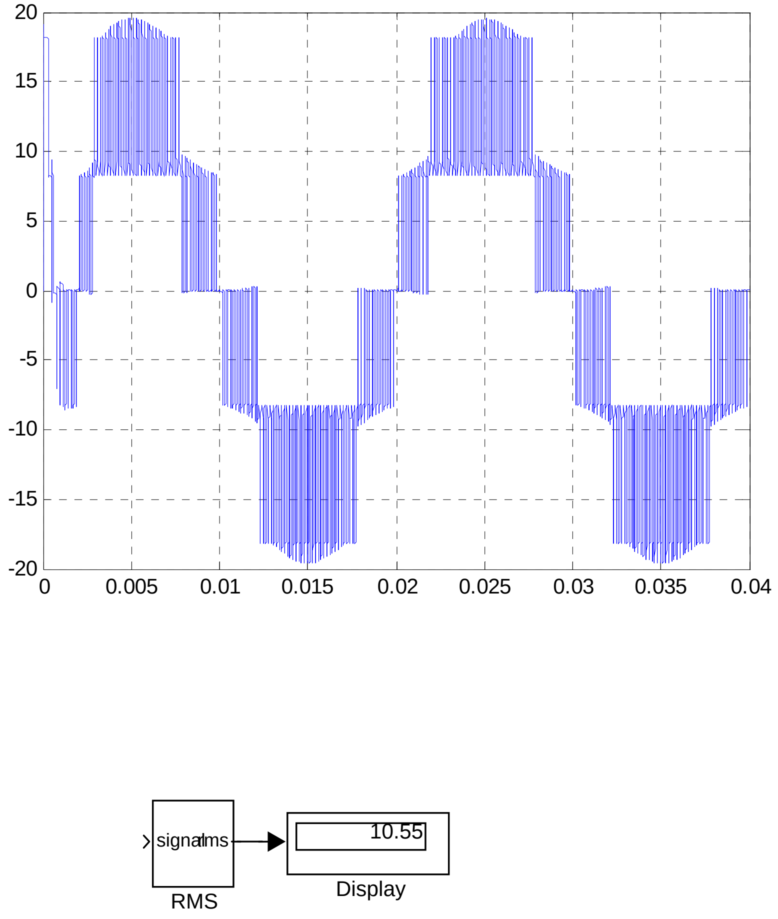


Fig 7.4 Output voltage waveform and output RMS value

A set-point of a sine wave with amplitude of 15V and RMS value of 10.61V is selected. As shown in Fig 7.4, the output voltage shown and the RMS value is been regulated by the PI controller to the desired value (set-point).

When very low $V_{control}$ is compared to a high frequency, a square pulse is produced. Thus, if the system maximum generating output voltage is 36V, and if the load only requires 12V, the number of PV arrays can be reduced since the advantage of the multilevel inverter is each inverter is in modular layout. Therefore able to add-on or replaced when necessary.

All the above simulation had met the solar powered generation system basic requirement. The ability to regulate the output voltage is made possible by PWM and PI controller.

8. Conclusion and recommendations

The objective of the project is to develop a renewable energy system using solar energy as the main source of energy. Cascaded H-bridge multilevel inverter with the synthesis of square-wave to form a step-like sinusoidal output voltage is selected due its numerous advantages as discussed in section 2.2.3. The basic requirement and concept is met for this project. The used of the ideal constant input dc source in the simulation is impractical if the inverter is meant for renewable energy source.

Thus, for future work, a cascaded H-bridge multilevel inverter model can be developed to investigate the quality of the output voltage waveform when PV array model is used as an input dc voltage source in the system.

In the simulation study of the square-wave switching technique, the only way to regulate the magnitude of the output voltage waveform is by adjusting the input dc source. This would require a costly dc-dc converter to be included in the system.

An inexpensive sinusoidal pulse width modulation technique is being introduced. Two methods of modulation technique has been discussed, Bipolar & Unipolar PWM method. Unipolar PWM is chosen in the next series of simulation studies due to its better output voltage waveform and THD. Improved type unipolar PWM had been developed to integrate with the PI controller due to its single control signal scheme. Pulse width modulation is able to cope with the variation of the load that is experienced by the power generation system.

A proportional-integral controller has been developed in the simulation study to adjust the peak amplitude of the control signal $v_{control}$, so that the modulation ratio varies accordingly to regulate the desired output voltage and RMS value.

The 5% Total harmonic distortion (THD) is not achieved in the 23 level multilevel inverter. Due to the non-linear decrease of the THD with the increment of the number of H-bridge module, it can be more economically to stop increasing the number of module and use alternative option to achieve the required THD. This may be develop in future work.

9. Critical Review and Reflection

Initial stage of gathering data from relevant books and IEEE Transactions shows great difficulty in understanding. Before project kick-start, seek help from tutor for better understanding on technique use on this project. That is pulse width modulation.

During the first usage on MATLAB program, advice from tutor is to use the simulink in MATLAB. It was observed to be a user-friendly program as help can be found in the program. In the first model trial-out is the 11-level square wave switching scheme. Signal builder was used as the switching signal to the inverter module. Manual calculations have to be done on the signal builder's square wave for the proper angle required. Though time-consuming and tedious, almost similar result obtained as compared to the IEEE Transaction explanation. When comes to harmonic analysis on the model, bottle-neck comes into play. It was difficult in finding the correct function to perform the harmonic analysis to the output waveform. After some reading in the sample model in help function, powergui function was tried and found to be successful.

For pulse width modulation stage, signal builder was tried for the carrier signal during the initial stage, but it was found only saw-tooth wave can be obtained instead of triangle wave. Furthermore, manual calculation becomes more complex when carrier frequency increases. It was found not practical to use signal builder. After seeking help from tutor, repeating sequence function was suggested to provide the required carrier waveform. Repeating sequence can be control more easily for the frequency changes. When comes to the comparator that required to compare the carrier signal and control signal, no sign of suitable function block found. Again seek help from tutor, which Relational operator was suggested. Single module for bipolar and unipolar switching technique was successfully built.

For the control technique for multiple modules use to obtain a step-like waveform was another bottle-neck when using pulse width modulation technique. After intense research on the paper on "A Comparative Modelling Study of PWM Control Techniques for Multilevel Cascaded Inverter," the shift control technique is implemented.

Highlighted by tutor that if only software simulation is inadequate for this project. A hardware need to be implemented as well to meet the academic level for a Capstone Project. Due to lack of time and difficulty in finding a suitable component for the pulse width modulation technique, it was given up. Future research on hardware implementation can be done base on own self interest.

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